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DESIGN, SIMULATION, AND PRELIMINARY TESTING OF A 20 AMPERE ENERGY MANAGEMENT SYSTEM

by

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June 2015

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The Department of the Navy is determined to find ways to increase the energy security of shore facilities. This is critical to ensure that facilities can meet fleet needs during a national crisis. An Energy Management System (EMS) using power electronics could be an important piece of this puzzle. In this thesis, a 20-ampere (A)-rated EMS module is designed and constructed that can be used for demonstrations and field testing. The prototype is used to conduct preliminary testing of the EMS over-current trip circuit. This thesis discusses the analog and digital redesigns that are needed to overcome the electromagnetic interference from the switching currents of the power modules that leak into the control circuitry. Finally, a Simulink model is designed to simulate the expected output from the H-bridge portion of the EMS. This model is tested and verified using measurements from the actual EMS prototype in the laboratory.

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DESIGN, SIMULATION, AND PRELIMINARY TESTING OF A 20 AMPERE ENERGY MANAGEMENT SYSTEM

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ABSTRACT

The Department of the Navy is determined to find ways to increase the energy security of shore facilities. This is critical to ensure that facilities can meet fleet needs during a national crisis. An Energy Management System (EMS) using power electronics could be an important piece of this puzzle. In this thesis, a 20-ampere (A)-rated EMS module is designed and constructed that can be used for demonstrations and field testing. The prototype is used to conduct preliminary testing of the EMS over-current trip circuit. This thesis discusses the analog and digital redesigns that are needed to overcome the electromagnetic interference from the switching currents of the power modules that leak into the control circuitry. Finally, a Simulink model is designed to simulate the expected output from the H-bridge portion of the EMS. This model is tested and verified using measurements from the actual EMS prototype in the laboratory.

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List of Acronyms and Abbreviations

AC	Alternating Current
A	Ampere
CNO	Chief of Naval Operations
DAC	Digital-to-Analog Converter
DC	Direct Current
DER	Distributed Energy Resource
DG	Distributed Generation
DS	Distributed Storage
DON	Department of the Navy
EMI	Electromagnetic Interference
EMS	Energy Management System
FPGA	Field-Programmable Gate Array
IGBT	Insulated-Gate Bipolar Transistor
JTAG	Joint Test Action Group
KCL	Kirchhoff's current law
KVL	Kirchhoff's voltage law
MPP	Magnetics Molypermalloy Powder
NPS	Naval Postgraduate School
PCB	Printed Circuit Board
PC	Personal Computer

PWM Pulse-width Modulation

SECNAV Secretary of the Navy

Executive Summary

Energy security at Department of the Navy (DON) shore facilities is a vital goal for national security [1]. These shore facilities must be ready to support the fleet when commercial power is not available [1]. The Secretary of the Navy (SECNAV) and Chief of Naval Operations (CNO) have established energy-management programs to ensure that the DON is able to meet these energy security goals [2], [3]. A method that could be used to ensure energy security is the use of microgrids that use a power-electronics based Energy Management System (EMS).

A 20 ampere (A) EMS prototype was designed and constructed that could eventually be used for demonstrations and remote site testing. The EMS was constructed using commercial insulated-gate bipolar transistor (IGBT) power modules, from STMicroelectronics, to implement the buck/boost converters and the H-bridge pulse-width modulation (PWM) inverter. These power modules include a smart shutdown feature that simplified the design of the over-current trip to ensure these power modules are not damaged [4], [5]. The smart shutdown will automatically shut off the IGBTs when the current goes over the current value that is set by a shunt resistor [4], [5]. Additionally, the shutdown module will send a fault signal to the field-programmable gate array (FPGA) that acts as the EMS controller. A second-order LC low-pass filter was designed and constructed to filter out the harmonics associated with the switching frequency of the H-bridge inverter.

Once the EMS printed circuit board (PCB) was constructed and turned on, it was discovered that there was electromagnetic interference (EMI) from the power modules switching on and off. The EMI was creating false over-current trip fault signals that were being sent to the FPGA. In an attempt to solve this problem, the value of the analog low-pass filter capacitor was increased. However, the larger filter had no real impact on the EMI issue. Two separate digital filters were created in the fault management portion of the FPGA that worked equally well. The first solution was to take three samples over a 480 ns period and ensure they were all positive for a fault condition before the controller would shutdown the EMS. The second method was to use a one-bit moving average filter, with a sample size of 32, to remove the noise. Over-current trip testing was conducted once the EMI issues were dealt with. The H-bridge power modules had trip points of 41.2 and 44.8 A, which

was lower than the desired trip points of 50-58 A. This was because the shunt resistance was higher due to resistance from the PCB traces.

A MATLAB Simulink model was created to simulate the H-bridge PWM inverter and LC filter output of the EMS. This model was then used to simulate the voltage and current waveforms of the output. These results were verified against the measured waveforms of the EMS prototype for both bipolar and unipolar voltage switching schemes. Additionally, the inductor current was simulated and compared against the measured waveforms. The inductor current waveforms, both simulated and measured, showed the ripple current being higher in frequency and reduced in magnitude when using unipolar voltage switching. This result is expected because the harmonics of a unipolar PWM inverter are the same as a bipolar inverter with double the switching frequency [6]. These higher harmonics allow for improved filtering by the LC low-pass filter.

List of References

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[6] N. Mohan, T. Undeland, and W. P. Robbins, *Power Electronics, Converters Applications and Design*, 3rd ed. New York: John Wiley and Sons, 2003, pp. 211–218.

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CHAPTER 1:
Introduction

The Department of the Navy (DON) is researching ways to increase energy security at its shore facilities, as this is critical to national security [1]. An Energy Management System (EMS) that uses power electronics may play a role in the solution. The design and construction of a 20-ampere (A)-rated EMS prototype is discussed in this thesis. A laboratory prototype is used to perform preliminary testing of the EMS over-current trip circuit. This thesis includes a discussion of how electromagnetic interference (EMI) issues were overcome with both hardware and software redesigns. A Simulink model of the H-bridge portion of the EMS will be designed to simulate the expected output. This model will be verified against the actual output of the EMS prototype.

The background and motivation of this project are discussed in this chapter. Next, the objective of the thesis and the approach will be discussed. Finally, the organization of the thesis is presented.

1.1 Background

Energy security is vital to ensure that DON shore facilities can meet the demands of the fleet [1]. The Secretary of the Navy (SECNAV) has established a program that will reduce dependence on commercial sources of power [2]. According to the Office of the Chief of Naval Operations (CNO), the commercial-power grid has an increased risk of going down at the same time that full naval assets would need to deploy [1]. The CNO has established a shore-energy management policy to ensure that the SECNAV's energy goals of energy security and use of alternative power sources are met [3].

One possible way to make DON shore facilities less dependent on commercial power is the use of EMS-driven microgrids. A microgrid is an isolatable power grid that has one or more distributed energy resources (DERs) and loads [4]. A DER can include distributed generation (DG) or distributed storage (DS) that can be used to provide power to the critical loads when commercial power is not available [4]. An EMS can be used to manage these resources to ensure that critical loads can maintain power during commercial power outages

[5]. It can also be used as a smart power meter that can provide reactive power and peak-power control [5]. Figure 1.1 illustrates how an EMS can be used with a microgrid. Here, the EMS is interfacing the local DGs and DS with the alternating current (AC) power grid to provide power to both critical and non-critical loads.

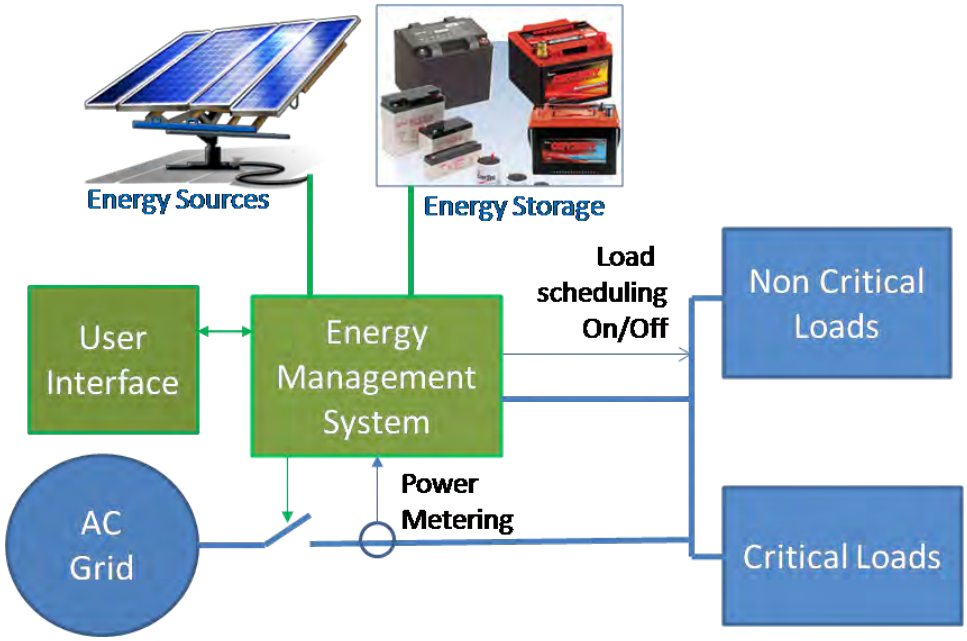

Figure 1.1. Block diagram of an microgrid using an EMS, from [6].

1.2 Objective

Previous work has been conducted at the Naval Postgraduate School (NPS) proving the viability and usefulness of the EMS technology utilizing a low-power field-programmable gate array (FPGA) based EMS [5], [7]–[12]. It is desired to design and construct a 20 A EMS prototype that can be transported and set up for the purposes of demonstrations and further studies at remote locations. The objective of this thesis is to design and construct this EMS unit, the over-current trip, and verify the proper output waveforms.

1.3 Approach

The 20 A EMS prototype was designed and constructed first. Second, a combination of analog circuits and digital control algorithms were used to get the over-current trip operational. The current trip was tested to verify that a fault would be reported and latched

when an over-current event occurs. Finally, a simulation model in Simulink was created and verified experimentally using the new EMS circuit.

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CHAPTER 2:
Energy Management System Overview

An overview of the functionality of a power electronics-based EMS is provided in this chapter. This chapter addresses EMS functions, including how the pulse-width modulation (PWM) works. Finally, common scenarios that illustrate the benefits of the system will be provided.

2.1 Energy Management System Functionality

A power electronics-based EMS can be used to provide an interface between any form of DER, such as solar cells, batteries, or a mechanical flywheel, with a local power grid [12]. The EMS monitors these resources and the status of the AC power grid. It makes decisions on how to provide and distribute these resources to ensure critical loads are constantly powered [5]. As an example, a basic EMS that links a battery to single phase AC power is shown in Figure 2.1. This is the basis for the EMS designed and constructed for the purpose of this thesis. For direct current (DC) to AC power conversion, the DC power provided by the battery has its voltage v_{batt} increased to the intermediate DC bus voltage v_{dc} by using the boost converter. This v_{dc} is then converted to AC voltage v_{ac} by using a PWM H-bridge inverter that is filtered and provided to the AC bus. How the PWM inverter works is discussed in Section 2.2. For AC to DC power conversion, v_{ac} is rectified to v_{dc} by using the H-bridge as a full-wave bridge rectifier. The buck chopper then reduces v_{dc} down to v_{batt} so that the battery can be charged. The controllers shown in Figure 2.1 take v_{ac} and v_{dc} along with logic from the desired values provided by the EMS logic and provides the necessary signals to the converters.

2.2 Pulse-width Modulation Inverter Operations

The PWM H-bridge inverter shown in Figure 2.1 has two sets of insulated-gate bipolar transistors (IGBTs) that are used as switches to convert DC voltage to AC voltage. To generate the output AC waveform, the IGBTs are switched on and off by comparing a voltage, with a triangular waveform v_{tri} at the switching frequency f_s, with a sinusoidal control voltage $v_{control}$ [14]. There are two methods in which the IGBTs pairs can switch: bipolar voltage switching and unipolar voltage switching.

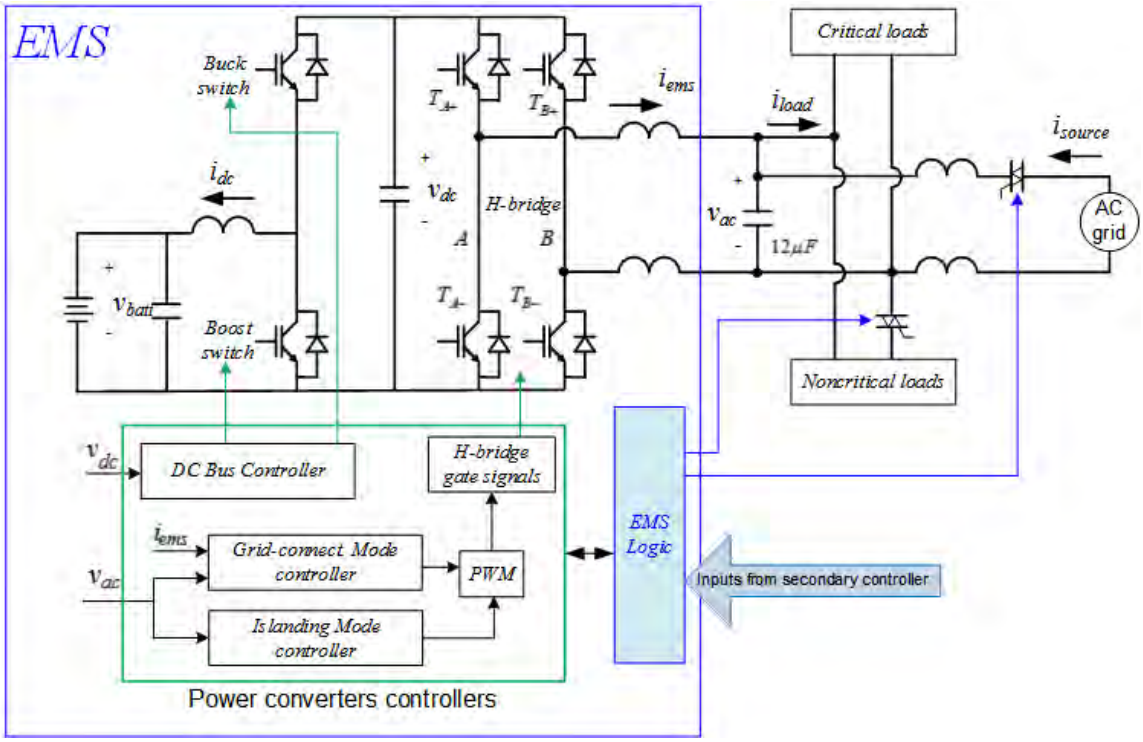

Figure 2.1. The basic topology of a power electronics-based EMS, from [13].

2.2.1 Bipolar Voltage Switching

For PWM bipolar voltage switching, the IGBTs are switched on and off in pairs that are diagonal to each other. In other words, IGBTs T_{A+} and T_{B-} from Figure 2.1 are switched on and off together, and T_{A-} and T_{B+} from Figure 2.1 are switched on and off together [14]. How these pairs are switched is illustrated in Figure 2.2. There is always one pair that is switched on at any given moment. A summary of how the IGBT pairs switch is shown on Table 2.1. When $v_{control}$ is above v_{tri}, the switching pair T_{A+} and T_{B-} is on and the other pair is off and the voltage across the output filter is v_{dc} [14]. Otherwise, the opposite is true. This method is called bipolar voltage switching because the voltage goes between v_{dc} and $-v_{dc}$ at every switching event [14]. The AC output LC filter removes the higher frequency harmonics associated with switching event to give v_{o1} shown in Figure 2.2.

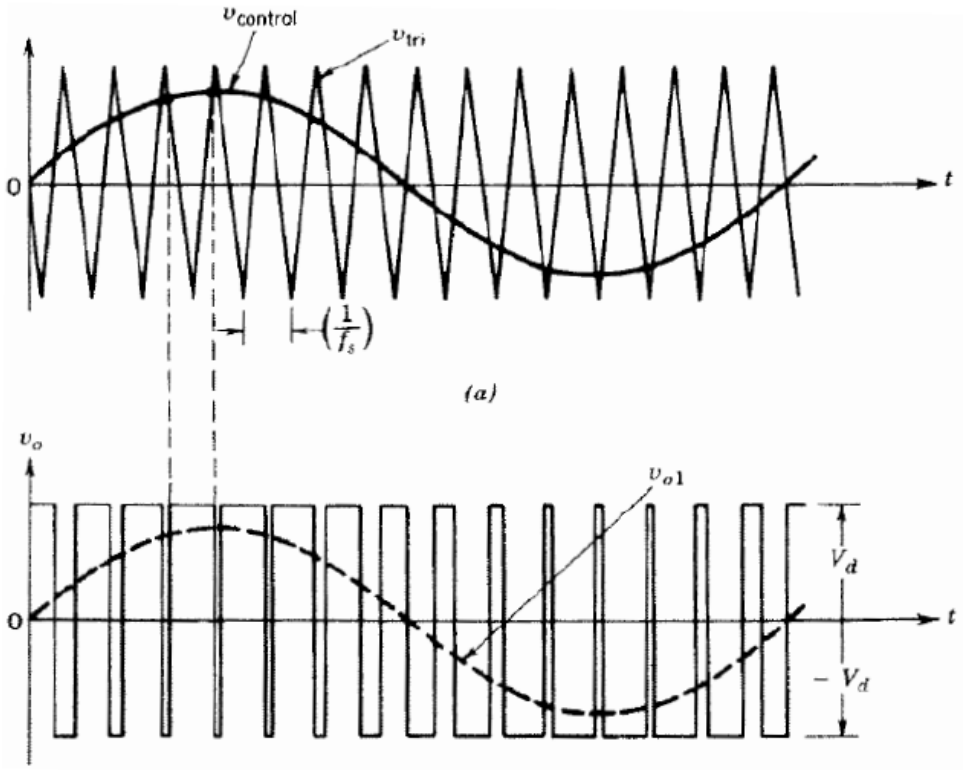

Figure 2.2. Voltage waveforms with bipolar PWM, from [14].

Table 2.1. The switching table for bipolar voltage switching, from [14].

$v_{control} > v_{tri}$	T_{A+} & T_{B-} On, T_{A-} & T_{B+} Off
$v_{control} < v_{tri}$	T_{B+}&T_{A-} On, T_{A+} & T_{B-} Off

2.2.2 Unipolar Voltage Switching

For unipolar voltage switching, each IGBT is switched individually based on a comparison of v_{tri} and two control voltages $v_{control}$ and $-v_{control}$ [14]. The IGBTs in leg A are controlled by $v_{control}$ and the IGBTs in leg B are controlled by $-v_{control}$ as shown by Figure 2.3 [14]. A summary of when each IGBT is turned on is shown in Table 2.2. From Figure 2.3, it can be seen that voltage across the output is the difference of v_{AN} and v_{BN} and that this voltage only varies from zero to $|v_{dc}|$. This switching method is called unipolar voltage switching for this reason. An advantage of this switching scheme is that the harmonics generated by the unipolar PWM inverter are the same as a bipolar PWM inverter operation at twice the

switching frequency [14]. The unipolar voltage switching method allows for more effective filtering by the AC output filter because the harmonics are at a higher frequency.

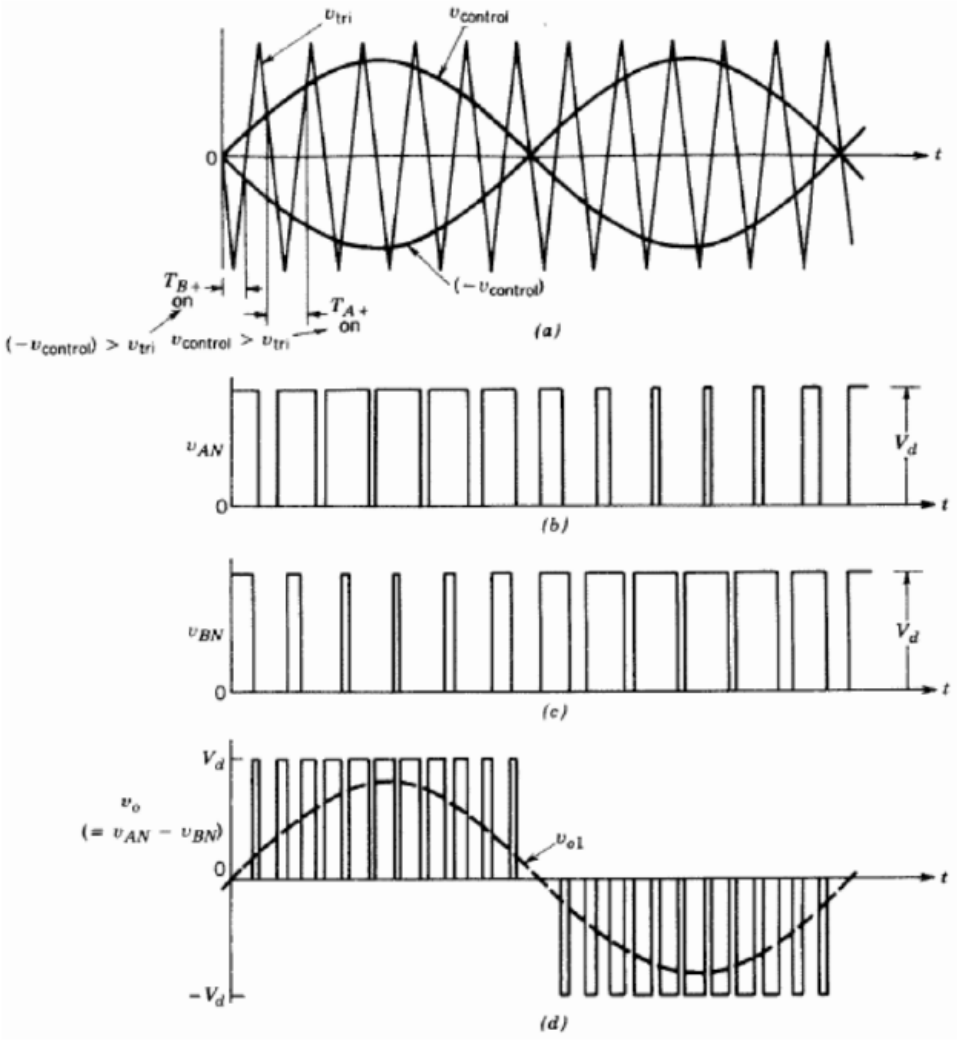

Figure 2.3. Voltage waveforms with unipolar PWM, from [14].

2.3 Energy Management System Scenarios

The benefits of cost savings and energy security that are provided by the EMS are demonstrated in the scenarios illustrated in Figure 2.4. The initial state of the EMS, as described by Oriti et al. [5], is that power to critical and non-critical loads is provided by the AC

Table 2.2. The switching table for unipolar voltage switching from [14].

$v_{control} > v_{tri}$	T_{A+} on	$v_{AN} = v_{dc}$
$v_{control} < v_{tri}$	T_{A-} on	$v_{AN} = 0$
$-v_{control} < v_{tri}$	T_{B+} on	$v_{BN} = v_{dc}$
$-v_{control} > v_{tri}$	T_{B-} on	$v_{BN} = 0$

source with the DC source in standby. In the first scenario they provide, the EMS is acting as a current source that uses the batteries to supply additional power to the loads when critical loading is increased. This example demonstrates the ability of the EMS to limit peak currents that have to be provided by the AC power grid. The second scenario in their illustration demonstrates the ability of the EMS to act as a voltage source to provide power to the critical loads during AC power grid outages. The final cited scenario demonstrates the ability of the EMS to shed non-critical loads as loading is increased to prevent going over power limits.

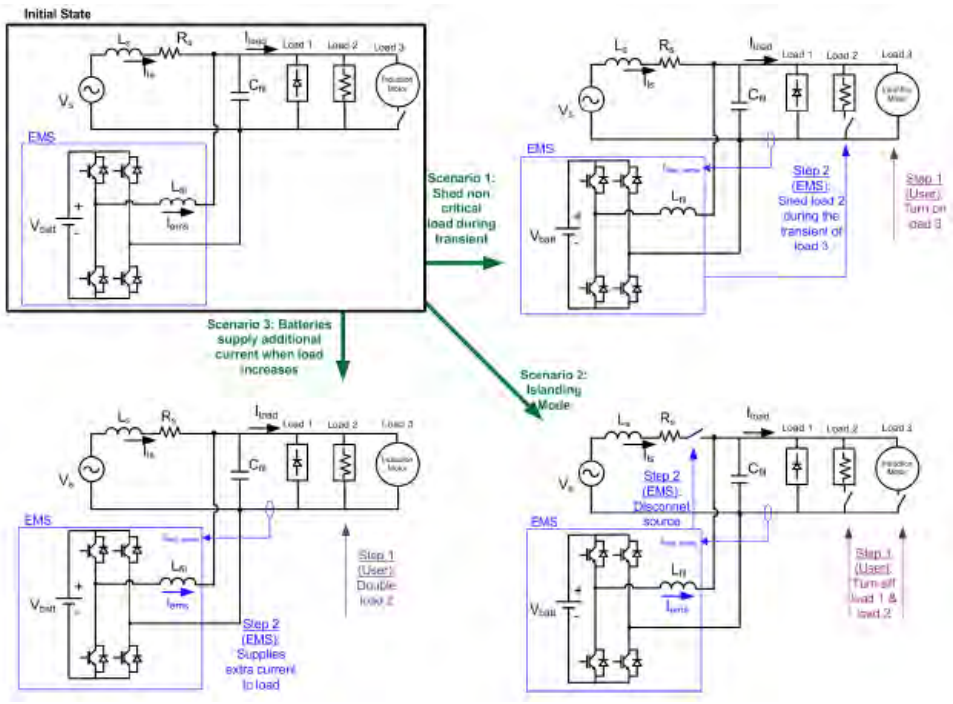

Figure 2.4. EMS scenarios used to demonstrate functionality, from [5].

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CHAPTER 3:
Energy Management System Prototype Hardware Selection

A new EMS prototype was designed that will eventually be able to demonstrate the functionality described in Section 2.1. This process involved determining how to implement the battery interface, the buck and boost converters, the H-bridge PWM inverter, the controller hardware, and the AC output filter that are illustrated in Figure 2.1. This prototype was designed and assembled at NPS in the lab. The first prototype that was constructed for testing is shown in Figure 3.1.

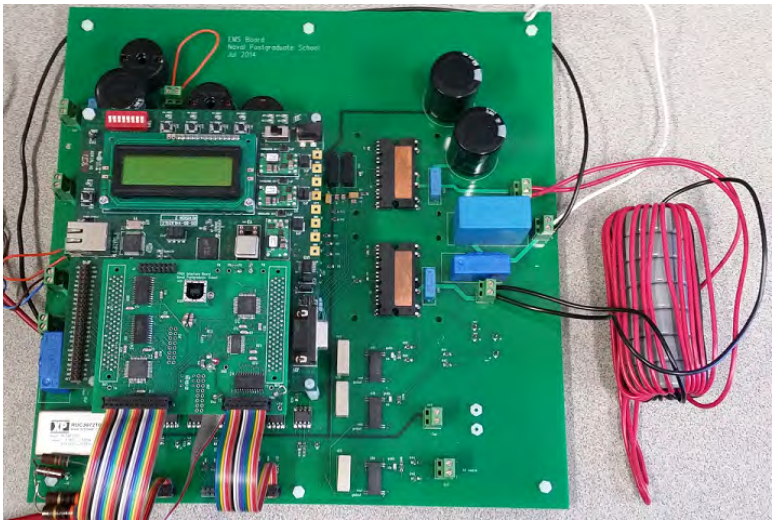

Figure 3.1. Image of the first 20 A EMS prototype.

3.1 Battery Interface

The EMS was designed with three separate battery interfaces to allow for the DC power storage capability that is required to power larger AC loads as needed. The system is scalable, as only one battery string is required to provide power to the control-circuit DC power supply. The maximum voltage rating of this power supply is 140 VDC, which limits the battery string voltage v_{batt} to this value. The inductance for each of the converter inputs

are provided by three 200μH inductors connected in series. There is a connection that can be used to attach an external inductor if needed. This connection allows additional inductance to be provided as needed for future testing along with keeping the weight down on the printed circuit board (PCB).

3.2 The Buck and Boost Converters

A 3-phase 18 A IGBT inverter module from STMicroelectronics [15] was used to provide the buck and boost converters. The key limits for the power module are shown in Table 3.1. This power module was selected because it provides for three buck/boost converters on one chip. A DC buck/boost converter has the same transistor layout as an individual leg of an inverter as shown in Figure 2.1. It requires different gate signals to drive the individual transistors as a buck/boost converter instead of generating a PWM AC waveform. Additionally, the module has an interlock feature that provides approximately 600 ns of dead time [15]. The dead time prevents both transistors from being turned on at the same time to minimize the chance of current shoot-through causing a short circuit. The built-in delay helps reduce the complexity of designing the controller as the on-off timing does not have to be handled by the controller software.

Table 3.1. Important specifications for buck and boost converter power module, from [15].

Parameter	Minimum	Maximum
Steady State v_{dc}		450 V
Surge v_{dc}		500 V
Continuous i_{dc}		18 A
Pulse i_{dc}		40 A
Power		52 W
Low Voltage Power Supply	-0.3V	21 V
Input Logic Voltage	-0.3 V	15 V
$V_{OD/\overline{SD}}$	-0.3 V	15 V
V_{ref}	0.5 V	0.58 V
V_{il}	0.8 V	1.1 V
V_{ih}	1.9 V	2.25 V

An important feature of this power module is the smart shutdown feature [15]. A simplified schematic of its operation is illustrated in Figure 3.2 [15]. The open-drain/shutdown

($OD/\overline{SD}$) pin must be pulled high to open-drain/shutdown voltage $V_{OD/\overline{SD}}$ so that the converter will run. The emitter current from the boost IGBT is converted to a voltage and measured by using the shunt resistor R_{shunt} and Ohm's law. The resulting voltage is then filtered through a RC low-pass filter to reduce the chance of false activation [15]. The filtered voltage is compared to the reference voltage V_{ref}. When the filtered voltage is higher than v_{ref}, the smart shutdown circuit immediately turns off all the power IGBTs in the module [15]. This feature provides immediate over-current protection for the module to prevent damage without having to worry about delays from the controller. At the same time, the transistor shown in Figure 3.2 is turned on. This causes $OD/\overline{SD}$ pin to be pulled low through the transistor as illustrated in Figure 3.3. The time that it takes for it to reach the low-logic level V_{il} is determined by the RC timing circuit shown in Figure 3.2. The RC circuit has a time constant of

$$\tau_1 \approx (R_{SD}||R_{internal})C_{SD} \tag{3.1}$$

where R_{SD} is the value of the pull-up resistor, $R_{internal}$ is the internal resistance in the smart shutdown feature, and C_{SD} is the capacitor to ground [15]. The pin voltage continues to decrease until the it reaches low-logic level V_{il}. Then the open-drain transistor is turned off, and the pin voltage slowly returns to $V_{OD/\overline{SD}}$ through a first-order RC circuit [15]. The RC circuit has a time constant of

$$\tau_2 \approx R_{SD}C_{SD} \tag{3.2}$$

where R_{SD} is the value of the pull-up resistor and C_{SD} is the capacitor to ground [15]. The delay from this circuit allows the shutdown signal to be read by the EMS controller, process it, and shutdown the power module. The internal protection is removed when the pin voltage reaches the high-logic level V_{ih} [15].

Values for R_{shunt}, R_{SD}, and C_{SD} had to be selected to implement this over-current protection. The value of 0.03 Ω was selected for R_{shunt} to give an over-current trip between 16.6 A and 19.3 A based on the variation of V_{ref} and Ohm's law. These values are to protect the device from a short-circuit fault while not interfering with normal operations with spurious trips. The values for R_{SD} and C_{SD} were selected to be 10.0 kΩ and 100 pF, respectively. By using

(3.2), τ_2 is calculated to be one μs. The operation of the over-current detection circuit will be shown in Section 4.1.

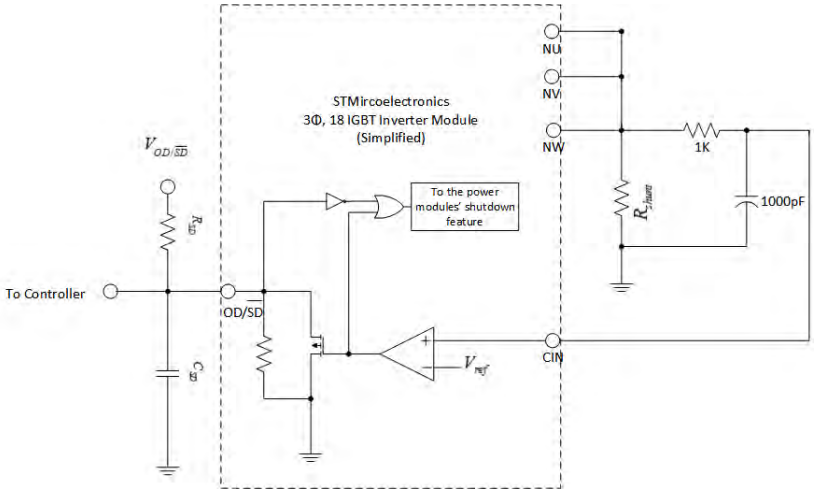

Figure 3.2. Simplified schematic of the smart shutdown feature of the buck/boost power module, based on [15].

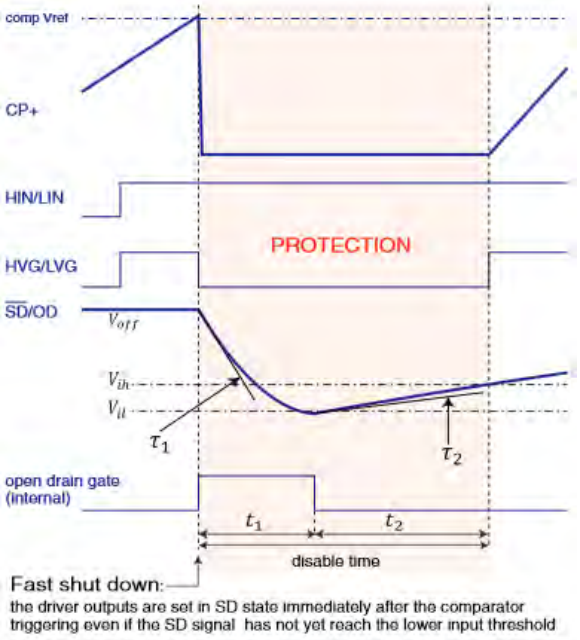

Figure 3.3. The timing for the smart shutdown feature, from [15].

3.3 The H-Bridge Inverter

Two single-phase 40 A IGBT power modules from STMicroelectronics [16] were used to implement the H-bridge as shown in Figure 2.1. The key limits for these power modules are shown in Table 3.2. For a 20 A rated AC circuit, the maximum steady-state peak current was calculated to be 28.3 A using

$$I_{peak} = \sqrt{2} I_{RMS} \tag{3.3}$$

where I_{RMS} is the RMS current. These power modules were selected because the 40 A current rating should be able to handle transients and reactive loading at peak power levels. An additional feature of these modules is that the input signals to the upper and lower IGBTs are driven by complimentary logic as shown in Table 3.3. First, the shutdown pin $\overline{SD}/OD$ is required to be pulled high to turn the converter on [16]. The upper IGBT will turn on when an active high logic signal is received while the lower IGBT will do the opposite [16]. This logic scheme means that the same signal from the controller can used to drive both of the IGBTs in a module as shown in Figure 3.4. The logic scheme simplifies the controller designs and reduces the number of control signals that must be sent to each module. The delay resistor R_{DT} connected between the DT pin and ground, shown in Figure 3.4, is used to prevent shoot-through fault. This resistor establishes a delay between one IGBT turning off and the other turning on as illustrated in Figure 3.5. The delay times DT_{LH} and DT_{HL} are set to be approximately 900 ns by making R_{DT} equal to 62 KΩ per the specification sheet [16].

These power modules also have the smart-shutdown feature that was discussed in Section 3.2. The main difference is that there is only one input to R_{shunt} versus the three inputs shown in Figure 3.2. The shutdown pins of these two modules are connected to the same R_{SD}, C_{SD}, and controller input as the buck/boost converter module discussed in Section 3.2. For the H-bridge power modules, two 0.02 Ω resistors are paralleled to make R_{shunt} equal to 0.01 Ω. The circuit should result in an over-current trip between 50 A and 58 A based on the variation on V_{ref} in Table 3.2. This trip should provide short-circuit protection while preventing spurious trips.

Table 3.2. Important specifications for the H-bridge power modules, from [16].

Parameter	Minimum	Maximum
Collector emitter voltage		600V
Continuous i_{dc}		40 A
Pulse i_{dc}		80 A
Power		100W
Low Voltage Power Supply	-0.3 V	21 V
Input Logic Voltage	-0.3 V	15 V
$V_{OD/\overline{SD}}$	-0.3 V	15 V
V_{ref}	0.5 V	0.58 V
V_{il}		0.8 V
V_{ih}	2.25 V	

Table 3.3. Truth table for H-bridge IGBTs, from [16].

Logic Input			Output	
Shutdown Pin ($\overline{SD}/OD$)	Lower IGBT ($\overline{LIN}$)	Upper IGBT (HIN)	Lower IGBT (LVG)	Upper IGBT (HVG)
L	X	X	Off	Off
H	L	H	Off	Off
H	H	L	Off	Off
H	L	L	On	Off
H	H	H	Off	On

Note: X: Input does not matter

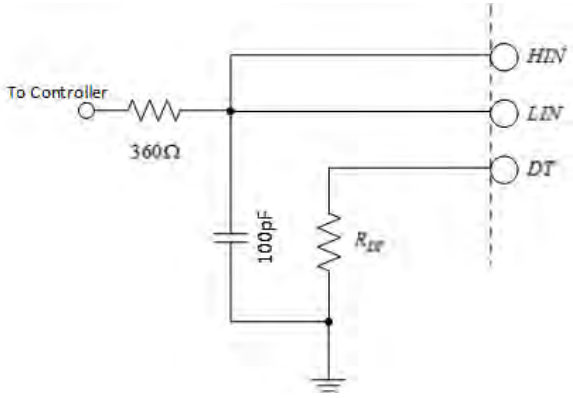

Figure 3.4. Simplified schematic of the H-bridge gate logic and dead time control.

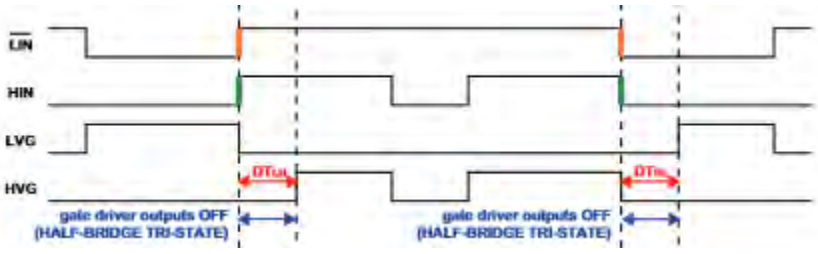

Figure 3.5. A timing diagram showing the delay caused by the delay resistor, from [16].

3.4 The EMS Controller

A Xilinx Virtex-4 LC development board from Memec was used to implement the controller for the EMS. This was the same board that was used in the previous EMS design. The development board features a Xilinx Virtex-4 LC FPGA that allows for rapid development and revision of the controller. A FPGA is an integrated circuit that allows the user to program its function as needed to perform different tasks [17]. The use of this board also allows the reuse of the programming from the previous design as a basis for the new controller. The Xilinx uses Simulink from MATLAB to develop a model of the functionality of the FPGA. The model created is then compiled by the Xilinx System Generator software to create VHDL code of the design. The Xilinx ISE Suite then takes the VHDL code and synthesizes the FPGA circuit design file. This design file is then uploaded to the FPGA through its Joint Test Action Group (JTAG) port using Xilinx's Chipscope software.

A simplified block diagram of how the FPGA interacts with the other parts of the EMS system to make up the EMS controller is shown in Figure 3.6. From Figure 3.6, it can be seen that the interfacing personal computer (PC) running Chipscope can be used to give commands to the FPGA through the JTAG-USB interface. The FPGA board then interacts with the EMS through the digital-to-analog converters (DACs) on the FPGA interface board that was previously designed. The resulting analog signals from the DACs are then electrically isolated and level shifted as necessary through the optocouplers. These signals provide command inputs to the buck/boost converters and the H-Bridge power modules. The voltage and current sensors, along with shutdown signals from the power modules, are then isolated and level shifted as necessary. The interface board then converts the analog signals into digital signals using the DACs. These signals are then feed back into the FPGA

so that it can monitor the various voltages and currents and make corrections as necessary. The FPGA can then communicate back with the controlling PC utilizing Chipscope.

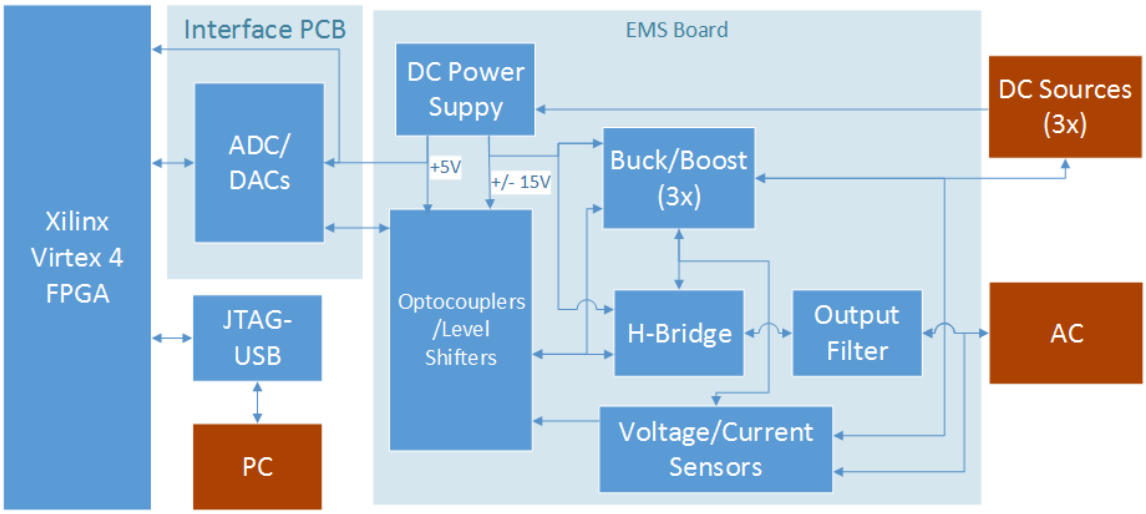

Figure 3.6. A simplified block diagram of the EMS controller.

3.5 AC Output Filter

The output voltage that is generated by the H-bridge must be filtered to remove the PWM-switching components while passing through the fundamental 60 Hz component. A second-order LC low-pass filter was used to accomplish this. The inductor is split into two parts as shown in Figure 2.1. This ensures the output AC voltage is balanced around the midpoint of the v_{dc} that is feeding the H-bridge. The corner or cutoff frequency for this filter can be determined by using

$$f_c = \frac{1}{2\pi\sqrt{LC}} \tag{3.4}$$

where L is the filter inductance and C is the filter capacitance. The desired corner frequency was selected to be three kHz as this is about one decade higher than the desired frequency of 60 Hz. It is also about one decade lower than the switching frequency of 17.5 kHz. This corner frequency provides enough separation from the desired 60 Hz component to allow it to pass without significant losses. While at the same time, the low-pass filter significantly reduces the harmonics associated with the switching frequency. The filter was designed by choosing a C of 12 μF and using (3.4) to determine L. The required L was determined to be 235 μH, which was divided into two inductors of 117 μH. The filter response was

simulated in LTSpice and is shown in Figure 3.7. This response allows the 60 Hz component through with no attenuation. There should be about 30 dB of attenuation for the 17.5 kHz harmonics associated with bipolar voltage switching. There should also be about 42.5 dB of attenuation of the 35 kHz harmonics associated with unipolar voltage switching. The inductors were created by winding wire around seven Magnetics Molypermalloy Powder (MPP) cores from Magnetics with an inductance factor A_L of 168 ± 13 nH/T^2 [18]. The minimum number of turns required can be determined by

$$N = \sqrt{\frac{10^3 L}{A_L}} \tag{3.5}$$

where L is in μH [18]. The minimum number of turns of 11 was determined by taking the worst case A_L of 155 nH/T^2 and inserting into (3.5).

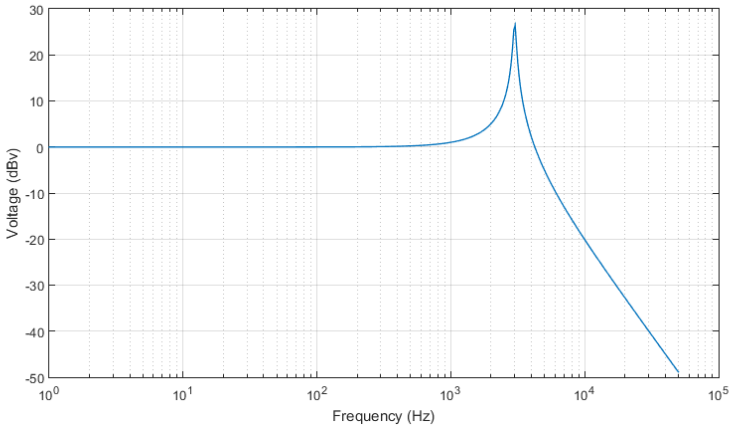

Figure 3.7. The simulated response of the output AC filter from LTSpice with a total inductance of 235 μH.

The actual inductors were created by winding two wires 13 times around a common core for better filtering. By rearranging (3.5) to form

$$L = 10^{-3} A_L N^2 \tag{3.6}$$

and inserting twice as many windings, it can be seen that the pair of windings has theoretically four times the inductance than would be expected for a single set of windings. The

combined inductance is reduced from the theoretical value by the mutual inductance between the two coils. The actual inductance values of the filtering inductors were measured and shown in Table 3.4. The expected range of the inductor values was calculated from (3.6) and is expected to be between 182.8 μH and 214.6 μH. The actual values from Table 3.4 are higher due to more flux is captured by the seven cores combined together. This core configuration is contrary to an assumption of (3.6) that each core is acting separately from each other. An expected corner frequency for the output AC filter can be solved by inserting the total inductance $L_1 + L_2$ into (3.4). The total inductance results in a corner frequency of 1490 Hz. The expected response was simulated in LTSpice and is shown in Figure 3.8. By comparing Figure 3.8 with Figure 3.7, it can be seen that the higher inductance has shifted the corner frequency to the left and improved the filter response to harmonics associated with the switching events. There is expected to be approximately 42 dB of attenuation of the 17.5 kHz harmonics associated with bipolar voltage switching and 55 dB of attenuation of the 35 kHz harmonics associated with unipolar voltage switching.

Table 3.4. The values of the two inductors in the output AC filter.

L_1	247μH
L_2	246μH
L_m	24.8μH
$L_1 + L_2$	950μH

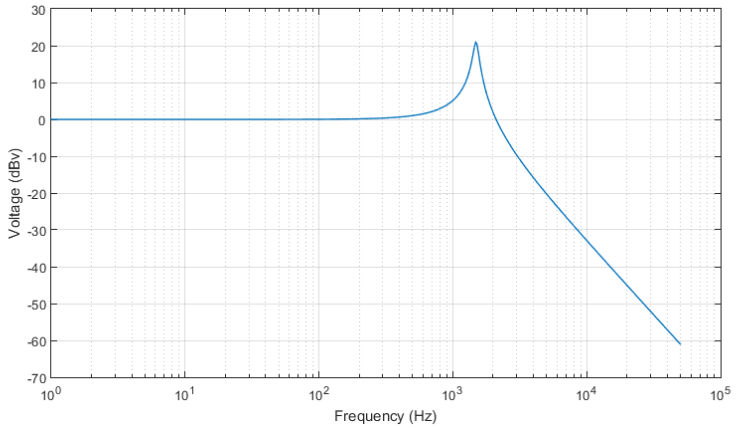

Figure 3.8. The simulated response of the output AC filter from LTSpice with a total inductance of 950 μH.

CHAPTER 4:
Electromagnetic Interference and Over-current Testing

Once the prototype was built based on the hardware designed in Chapter 3, it was desired to conduct over-current testing of the H-bridge PWM power modules. This chapter discusses the EMS controller enable and shutdown circuit and the EMI issues that had to be addressed to make the over-current trip function. Additionally, the chapter discusses the process used to conduct the over-current trip test along with the results of these tests.

4.1 Energy Management System Controller Enable and Shutdown Circuit

The Simulink schematic of the enable and shutdown circuit is shown in Figure 4.1. The FPGA is set to run at a 25 MHz clock speed which means that there is a clock cycle every 40 ns. To enable the EMS, the circuit checks that the on/off signal is inputted from the user's PC Chipscope interface goes from low to high. It does this by performing

$$y[n] = x[n] \,\&\, !x[n-1] \tag{4.1}$$

where $y[n]$ is the output of the operation, $x[n]$ is the current sample, and $!x[n-1]$ is the inverted previous sample. The output from this operation causes the set-reset flip-flop output to become true. The flip-flop output sets the enable output to high which causes the $V_{OD/\overline{SD}}$ to go to high. The enable output drives the $OD/\overline{SD}$ pin to high as discussed in Section 3.2 and Section 3.3. An over-current fault is detected by checking for a high-to-low transition of the over-current fault labeled $data4a\_fault$ in Figure 4.1. The high-to-low transition is determined by

$$y[n] = !x[n] \,\&\, x[n-1] \tag{4.2}$$

where $!x[n]$ is the current sample inverted. This transition is checked for because the signal that is sent from the smart-shutdown feature is pulled low upon over-current detection as shown in Figure 3.2. The fault signal resets the set-reset flip-flop to false and sets the enable output to low. The enable output sets $V_{OD/\overline{SD}}$ to zero and keeps the power modules

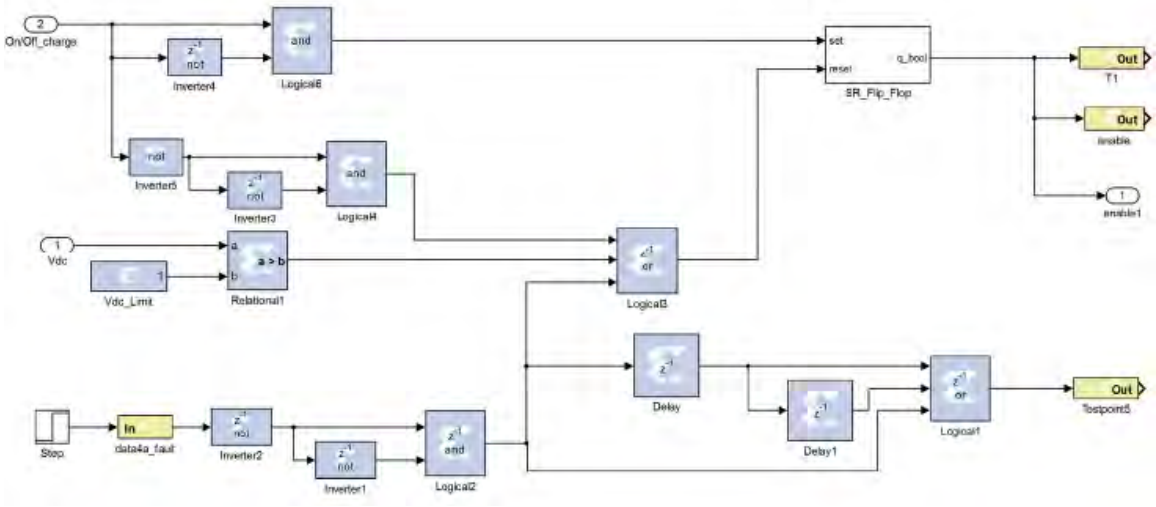

Figure 4.1. The original fault management circuit design in Simulink.

off. Additionally, the modules are shutdown if the on/off signal is set to off or if v_{dc} goes above its limit which is not in the scope of this thesis.

4.2 Electromagnetic Interference Issues

When the EMS was first started with the controller over-current protection described in Section 4.1 enabled, the EMS would immediately shutdown. It was found that the voltage from EMI on the $OD/\overline{SD}$ pin was causing false over-current trips. The pin voltage was measured and is shown in Figure 4.2. This over-current trip was not a real fault because when the over-current fault detection was disabled in the controller, the EMS operated as expected with no faults. If there had been a real fault, the smart-shutdown feature would have shut off the effected power modules for 1-2 ms as explained in Section 3.2 which never occurred. The EMI is believed to be caused by large currents spikes from the IGBT switching events.

Several strategies were attempted to try to mitigate the EMI problem. The first was to try to solve it by increasing C_{SD} to 1000 pF in attempt to filter the noise out. The result from the change is shown in the Figure 4.3. The change to C_{SD} had the side effect of increasing τ_2 to 10 μs. This change had very little to no effect on the voltage from EMI. From this observation, it is believed that the source of the EMI injection into the circuit is due to

the switching currents being present on the ground side of the C_{SD}. The currents are there because the ground side of C_{SD} has more than one return path to the analog ground [19]. The grounding issue can only be handled by a redesign of the prototype board. Another solution must be used to continue testing of this prototype. Therefore, two different and equally viable changes to how the FPGA handles the over-current fault management were made in an attempt to eliminate the false trips.

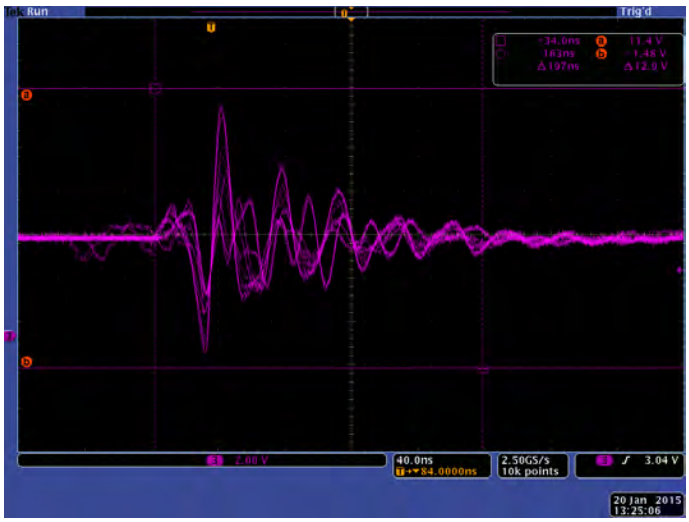

Figure 4.2. The voltage on the $OD/\overline{SD}$ pin during a switching before increasing C_{SD}. The time and voltage scale is 40 ns and 2 V per unit, respectively.

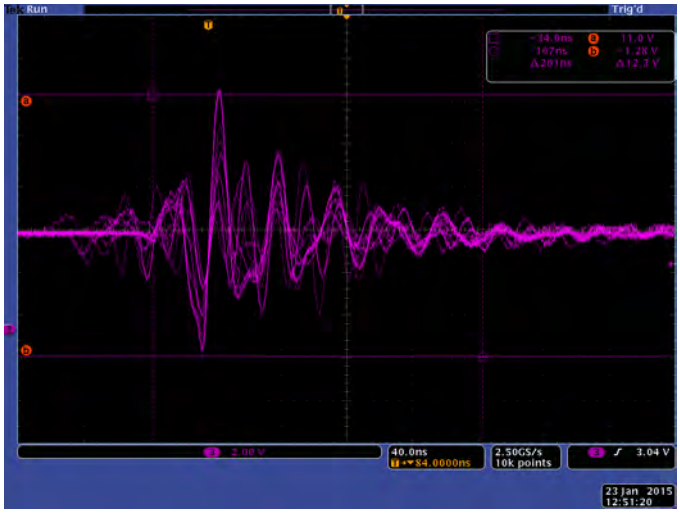

Figure 4.3. The voltage on the $OD/\overline{SD}$ pin after increasing C_{SD} to 1000 pF. The time and voltage scale is 40 ns and 2 V per unit, respectively.

4.2.1 Multiple Sample Fault Detection

From Figure 4.3, it can be seen that the EMI transient is approximately 500 ns long. A false trip should be avoided if multiple fault signals are required over this time period. Therefore, the first digital method was to change the fault detection circuit to take multiple samples as shown in Figure 4.4 and Figure 4.5. The $data4a\_fault$ is first inverted as shown in Figure 4.4 and sent to the subsystem shown in Figure 4.5. The subsystem then samples the line every 4 clock cycles or every 160 ns by using the a two bit free running timer *Counter*. Every time that the *Counter* resets to zero, it causes each register to store the current value of the previous register. These registers are logically ANDed together so that it is only true if all three are positive. The result of this means that a fault is registered if and only if a fault detection has occurred during those three samples. The samples are taken over a 480 ns period to ensure that any switching noise has died down. The resulting output is compared to the previous sample in accordance with (4.1) to ensure a low-to-high transition occurs. The low-to-high transition signifies that an over-current trip has occurred. Once the filter was implemented, the spurious shutdowns of the EMS system decreased to a minimal amount.

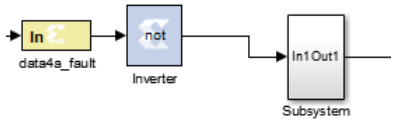

Figure 4.4. The new fault protection input stage with inverter going into the new filter subsystem.

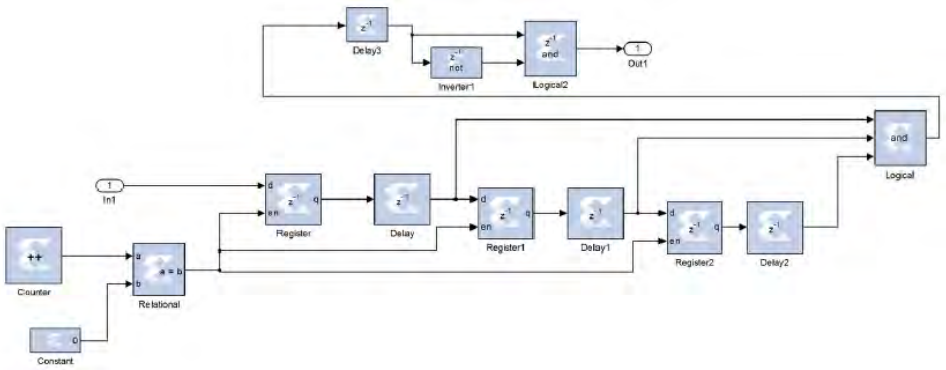

Figure 4.5. The first new fault detection circuit to overcome the EMI issues.

4.2.2 One-Bit Moving Average Noise Filter

The second digital method used was a moving average digital filter because they are a common and simple way to remove noise [20]. The output of the generic moving average filter $y[n]$ can be described by

$$y[n] = \frac{1}{M} \sum_{i=0}^{M-1} x[n-i] \tag{4.3}$$

where M is the number of samples and $x[n-i]$ is the i^{th} previously sampled input [20]. The actual output $y_{actual}[n]$ can be found using

$$y_{actual}[n] = 1 : \qquad y[n] \geq 0.5 \tag{4.4}$$

$$y_{actual}[n] = 0 : \qquad y[n] < 0.5 \tag{4.5}$$

where $y[n]$ is rounded using normal rounding rules to get a one bit output. Now (4.3) can be substituted into (4.4) and (4.5) to get

$$y_{actual}[n] = 1 : \qquad \sum_{i=0}^{M-1} x[n-i] \geq \frac{M}{2} \tag{4.6}$$

$$y_{actual}[n] = 0 : \qquad \sum_{i=0}^{M-1} x[n-i] < \frac{M}{2} \tag{4.7}$$

to change the division into a comparator operation.

The equations (4.6) and (4.7) could be implemented by the FPGA by performing $M-1$ summing operations and comparing the result to $M/2$. However, the filter can be implemented in a more efficient manner. This can be done by rewriting (4.3) to

$$y[n] = \frac{y[n-1] + x[n] - x[n-M]}{M} \tag{4.8}$$

so that it is based on the previous output $y[n-1]$, the next input $x[n]$, and the oldest input $x[n-M]$ in the buffer. Since $x[n]$ and $x[n-M]$ can only be either 0 or 1, $y[n]$ can only be different by 0, 1, or -1 from $y[n-1]$ as shown in Table 4.1. The resulting function can be implemented with an Xilinx FPGA by using a up/down counter with an active high enable port as shown in Figure 4.6. To make the counter work, Table 4.1 is translated in the counter

truth table shown in Table 4.2. The *up* port sets the direction of the counter and *en* is the enable port.

Table 4.1. How the output of the moving average filter changes with regards to the next input and oldest value in buffer.

$x[n]$	$x[n-M]$	$\Delta y[n]$
0	0	0
1	0	+1
0	1	-1
1	1	0

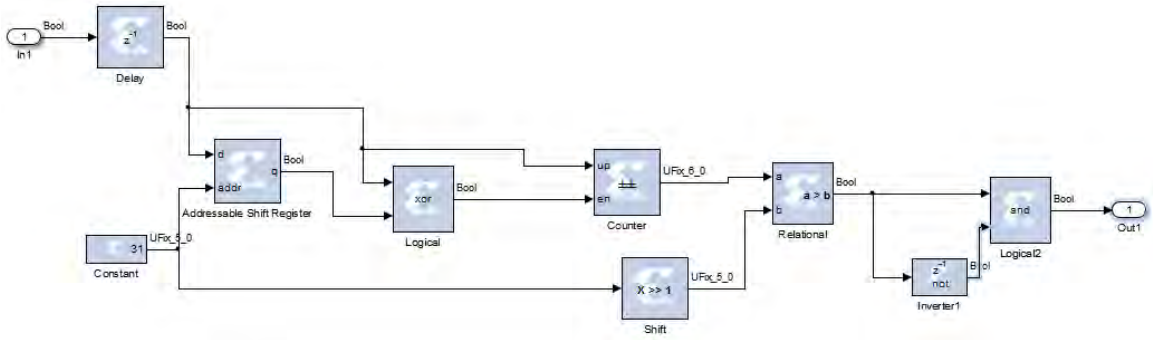

Figure 4.6. A new fault detection circuit based on an one bit moving average filter.

Table 4.2. The truth table to implement the moving average counter in Xilink.

$x[n]$	$x[n-M]$	up	en
0	0	X	0
1	0	1	1
0	1	0	1
1	1	X	0

X: Input Does Not Matter

From Table 4.2, the logic needed to drive each port is

$$up = x[n] \tag{4.9}$$

$$en = x[n] \oplus x[n-M] \tag{4.10}$$

where $\oplus$ is the XOR logic function, $x[n]$ is the output of the delay at the input, and $x[n-M]$ is output of the shift register in Figure 4.6. The delay on the input is to ensure metastability of the subsystem to ensure that all bit transitions occur predictably. The output of the delay is fed into the XOR gate and the addressable shift register. The addressable shift register is used to create an adjustable shift register that delays its output by $addr+1$ and feeds this value into the XOR gate. The output of the XOR gate is used to enable the counter in accordance with (4.10). The direction of the counter is selected by reading the output of the delay in accordance with (4.9). The constant that is used for $addr$ is set to $M-1$ to create the proper filter size that can be easily changed as necessary. The constant is right shifted by one bit to perform a low-cost divide-by-2 where the result is rounded down to the nearest integer. The right shift operation was used as opposed to a division function to reduce the amount of resources required. The approximation should work equally as well for the filter. Here the comparator implements

$$y_{actual}[n] = 1: \qquad \sum_{i=0}^{M-1} x[n-i] > \frac{M-1}{2}(rounded\,down) \tag{4.11}$$

$$y_{actual}[n] = 0: \qquad \sum_{i=0}^{M-1} x[n-i] \leq \frac{M-1}{2}(rounded\,down) \tag{4.12}$$

where the left side of the equation is the output of the counter and the right side is the output of the right shift function to approximate (4.6) and (4.7). The output of the comparator is checked for a low-to-high transition that is outputted to the fault management circuit discussed in Section 4.1.

A filter size M was set to 32 samples to filter out the EMI from the $data4a\_fault$. This size was selected to ensure that there is fault detected in at least 16 samples over a 1.28 μs period. The EMI has the potential of causing approximately 13 samples to be falsely positive over the same time period. The sample size should minimize the chance that the EMS is shutdown from a false positive signal. There were minimal shutdowns when this filter was implemented. Therefore, it performed as equally as well as the filter discussed in Section 4.2.1. The filter has the ability to be further adjusted for faster response by reducing the size of M. This reduction would be a trade off as the chance for shutdown from false positives would increase and is unnecessary at this time. The smart-shutdown

feature discussed in Section 3.2 protects the power devices and keeps the shutdown signal latched for at least 1-2 μs.

4.3 Over-current Testing

The over-current trips of the H-bridge power modules were tested by intentionally keeping on one of the inverter switching pairs. This allows current to conduct in one direction through the load to the other leg. The current flow through the load allows i_{ems} to build up until it rises high enough through R_{shunt} to produce a voltage higher that V_{ref}. This will trip the smart-shutdown feature as described in Section 3.2 and Section 3.3. The current i_{ems} was measured throughout the test to determine the peak current reached when the trip occurs. The enable signal was monitored to observe the EMS controller response to the trip. Additionally, v_{dc} was monitored for transients during the testing.

The over-current fault generation event for current flow from the *A* H-bridge power module to the *B* module is demonstrated in Figure 4.7. The maximum value that the current reaches indicates the over-current trip set-point for the *B* power module during a short-circuit fault. The test was repeated with a current flow from the *B* H-bridge module to the *A* bridge module as shown in Figure 4.8. This test gave the over-current trip set-point for the *A* module.

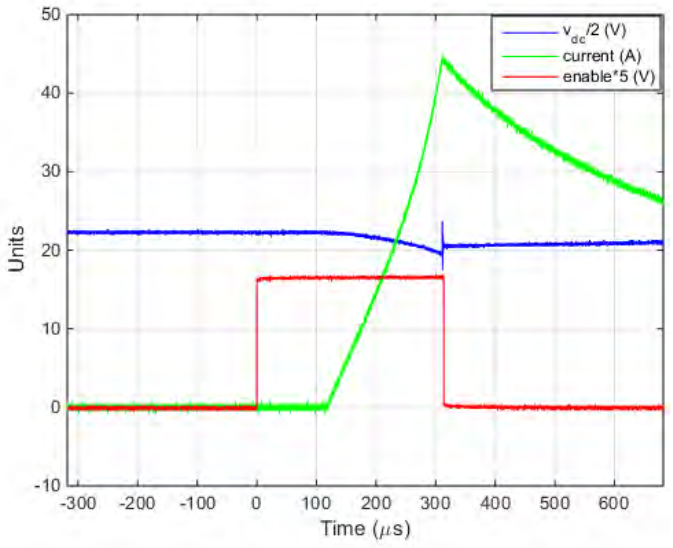

Figure 4.7. The voltage and current waveforms for current flow from power module *A* to *B*.

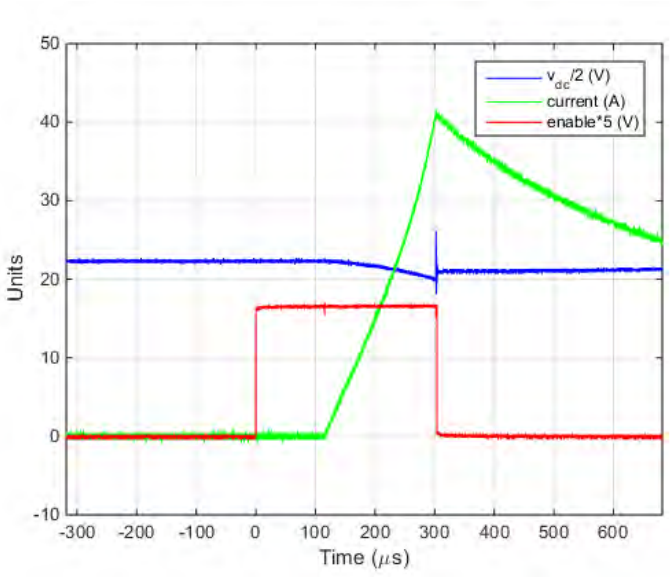

Figure 4.8. The voltage and current waveforms for current flow from power module B to A.

A summary of these results for the over-current testing is shown in Table 4.3 along with the expected values of the trip set-points. The results indicate that both trips are considerably below expected trip value of 50-58 A. The resulting set-points limits the EMS ability to handle transient loading. The reduced values are most likely due to R_{shunt} being greater than the designed value because of the resistance of the PCB copper traces. The results are also shown in Table 4.3 where the calculated R_{shunt} is predicted from Ohm's law and V_{ref}. The actual trip set-point is very sensitive to the actual value of R_{shunt} as shown in Table 4.3. These trace resistances could be reduced in the future PCB designs by increasing the PCB trace widths and reducing their lengths.

Table 4.3. Summary of results for over-current testing.

Module	Expected trip value (A)	Actual trip value (A)	Designed R_{shunt} Ω	Calculated R_{shunt} Ω
A	50-58	41.2	0.01	0.012-0.014
B	50-58	44.8	0.01	0.011-013

To focus on the over-current transient and controller response, a blown up view of Figure 4.7 is shown in Figure 4.9. From this figure, it can be shown that there is about a 2.8

μs delay before the controller turns off the enable signal. This delay is acceptable as the purpose of the controller shutting down the EMS is to prevent overheating due to cycling of the over-current event. The immediate protection of the power modules come from the smart-shutdown feature discussed in Section 3.2 and Section 3.3.

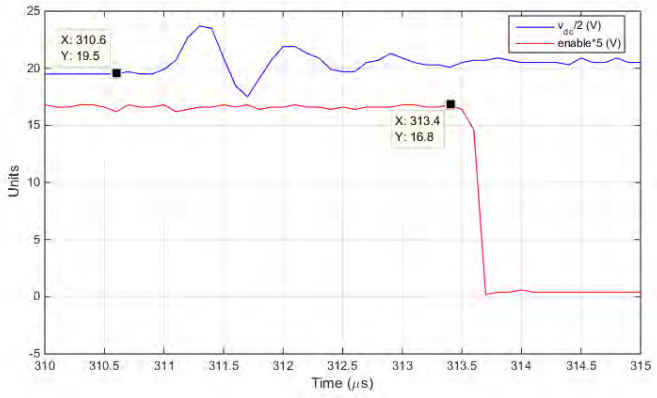

Figure 4.9. A blown up view of v_{dc} and the enable pin showing the controller delay.

CHAPTER 5:
Simulink Voltage Waveform Simulation and Verification

The generation of a Simulink simulation of the PWM H-bridge inverter and AC output filter stages of the EMS will be discussed in this chapter. This discussion will include how the PWM section and the output filter and load will be simulated. Additionally, the simulation will be verified against the actual AC waveforms of the prototype.

5.1 Simulink Model Overview

The Simulink model was created to simulate the inverter output stage shown in Figure 5.1. The output stage in Figure 5.1 was based on past work conducted using the previous-generation EMS [12]. Here the H-bridge of the EMS is connected to a simple resistive load through its AC output filter. This configuration allows for a simple simulation to be designed that can be built upon to include additional features. The loss resistor R_{loss} has been added so that losses in the output stage can be simulated as necessary [12]. The top level block diagram from Simulink is shown in Figure 5.2 which is based on previous work [12], [21]. Here the simulation is broken up into three separate subsystem blocks to break apart the functionality. These subsystems make it easier to update and upgrade each separate system. Additionally, the $v_{control}$ sine wave generator and the v_{dc} source are also on this diagram. The control voltage $v_{control}$ has an amplitude of 0.832 which mimics the prototype's v_{ref} amplitude. There is a constant PWM_mode to allow the model to switch from bipolar to unipolar voltage switching.

5.2 Pulse-width Modulation Simulation

The subsystem of the Simulink model that generates the PWM control signals is shown in Figure 5.3 [12], [21]. Here a sine wave generator, with the switching frequency of 17.5 kHz, is used to generate the triangle wave by taking the inverse sine of the value generated [12]. The result is a linearly increasing and decreasing line between $-\pi/2$ and $\pi/2$. The range will be reduced to value between -1 and 1 using the gain multiplier of $2/\pi$. For bipolar

voltage switching, the triangle signal will be logically compared to $v_{control}$ and the resulting signal is sent to the legs A and B per Table 2.1. For unipolar voltage switching, the triangle signal is compared to $v_{control}$ and $-v_{control}$ and sent to the H-bridge legs per Table 2.2.

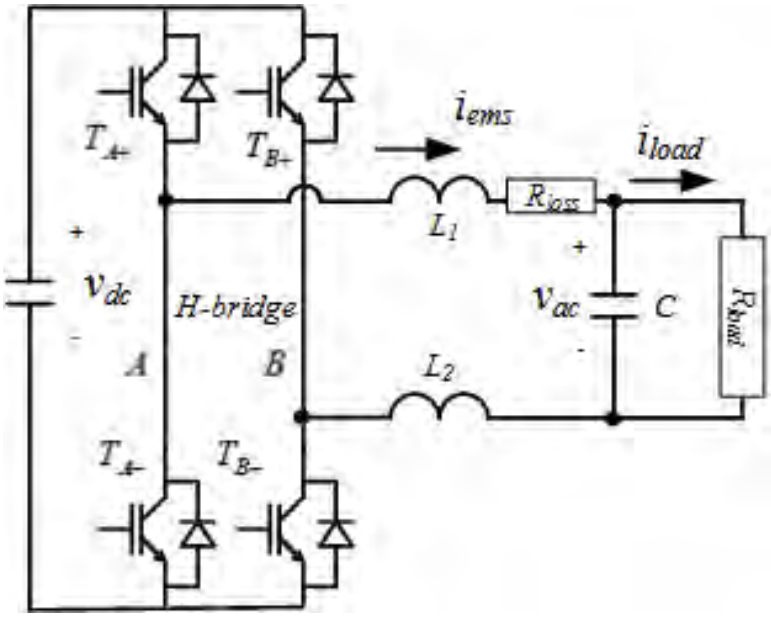

Figure 5.1. The EMS output stage with a simple resistive load.

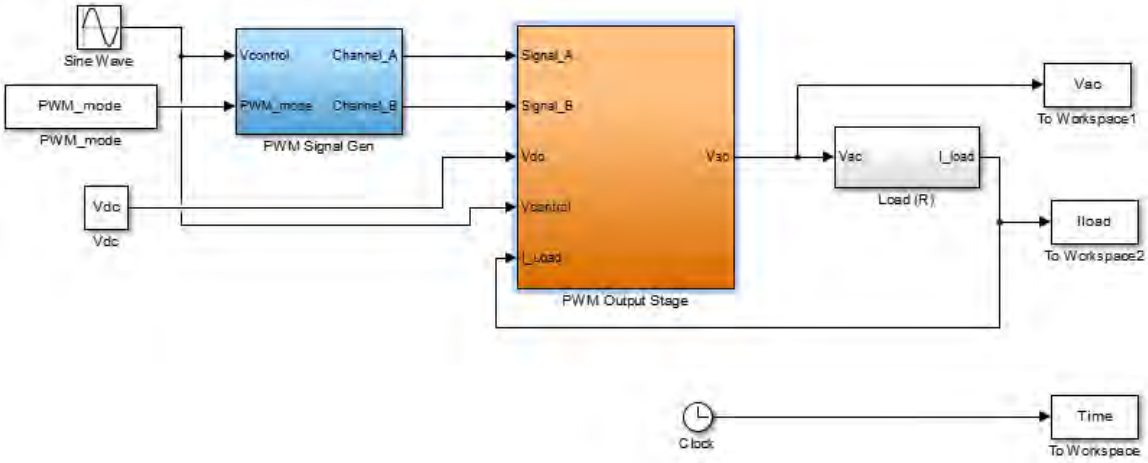

Figure 5.2. An overview diagram of the Simulink EMS Model, based on [12], [21].

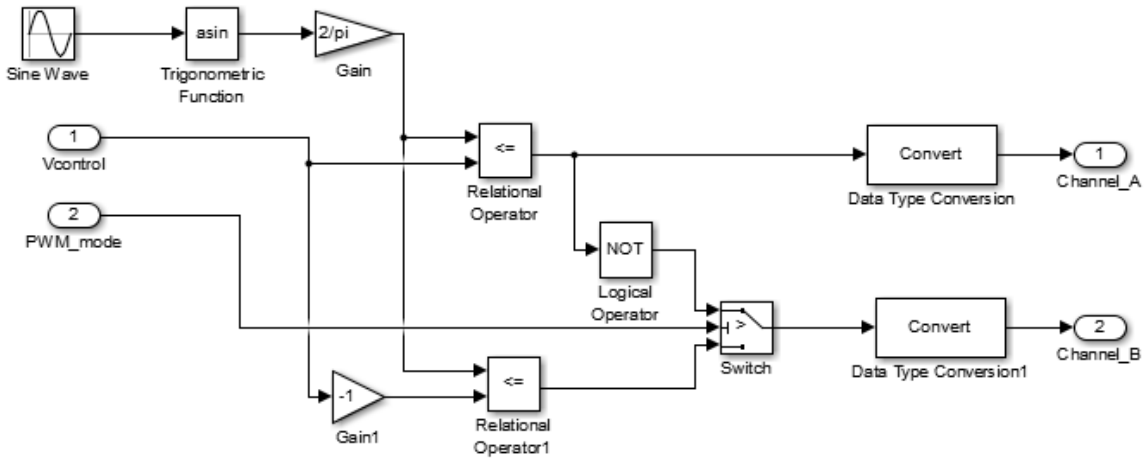

Figure 5.3. The PWM signal generation subsystem for the Simulink Model, based on [12], [21].

5.3 AC Output Filter and Load Simulation

Kirchhoff's voltage law (KVL) around the AC output filter and Kirchhoff's current law (KCL) at the output of the filter were used to generate the necessary mathematical model from Figure 5.1. This analysis resulted in

$$V_{dc} - (L_1 + L_2)I_{ems}s - V_{ac} - V_{R_{loss}} = 0 \tag{5.1}$$

and

$$I_{ems} = I_C + I_{load} \tag{5.2}$$

in the Laplace domain [12]. The filter-inductor current I_{ems} can be determined by rearranging (5.1) to get

$$I_{ems} = \frac{V_{dc} - V_{ac} - V_{R_{loss}}}{Ls} \tag{5.3}$$

where L is the filter inductance and $V_{R_{loss}}$ is the voltage drop due to the losses [12]. The AC output voltage V_{ac} can be solved for by using (5.2) and

$$V_{ac} = \frac{I_C}{sC} \tag{5.4}$$

to get

$$V_{ac} = \frac{1}{sC}(I_L - I_{load}) \tag{5.5}$$

where C is the capacitor value, and I_{ems} and I_{load} are currents shown in Figure 5.1 [12]. The loss-voltage drop $V_{R_{loss}}$ is determined to be

$$V_{R_{loss}} = R_{loss} I_{ems} \tag{5.6}$$

and load current is calculated by

$$I_{load} = \frac{V_{ac}}{R_{load}} \tag{5.7}$$

using Ohm's law.

The PWM-simulation output subsystem is shown in Figure 5.4 is based on [12] and [21]. Here *Signal_B* is subtracted from *Signal_A* to get either a 1, 0, or -1. The result is multiplied by $V_{dc} - 2V_{drop}$, where $2V_{drop}$ is the voltage drop due losses in the IGBTs, to get either $-(V_{dc} - 2V_{drop})$, 0, or $V_{dc} - 2V_{drop}$ [12], [21]. The resulting outcome simulates the output of the H-bridge. The output filter takes (5.3), (5.5), and (5.6) and implements them in Simulink block format. The Load (R) subsystem shown in Figure 5.5 implements (5.7) and feeds back I_{load} back to the filter simulation. This model is designed to output the voltage before the filter v_{ems}, i_{ems}, v_{ac} , and i_{load} as needed. There is a switch in Figure 5.4 to cut out the simulation of the switching events. This switch facilitate faster simulations when the switching events are not required for simulation.

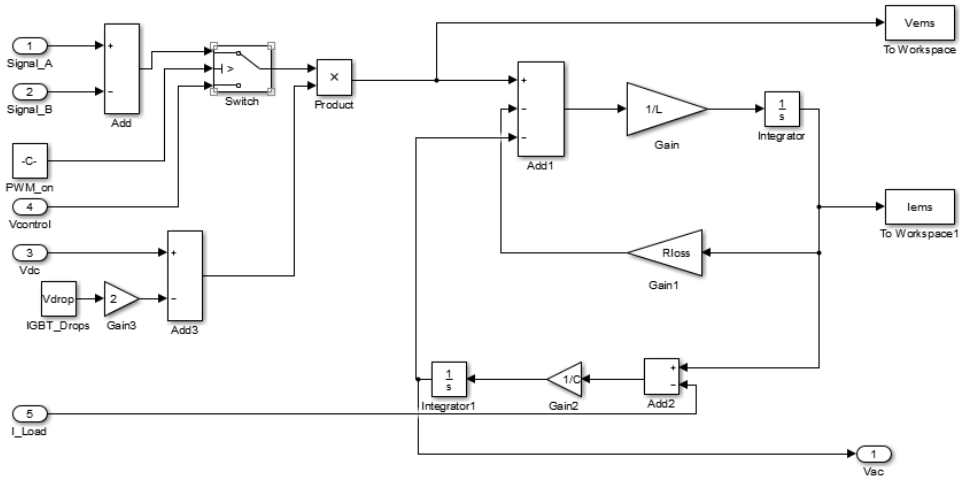

Figure 5.4. The PWM output stage subsystem in Simulink, based on [12], [21].

Figure 5.5. The load (R) subsystem in Simulink to simulate the resistive load.

5.4 Simulink Model Results and Comparison

The v_{ac} and i_{load} of the EMS prototype was measured while supplying a 100Ω load in PWM bipolar voltage switching mode which is shown in Figure 5.6. Here the maximum output voltage and current was measured to be 31 V and 0.375 A, respectively, with a DC supply voltage of 42V. The model was used to simulate bipolar voltage switching. Table 5.1 summarizes the parameter values used in model and their sources. The simulation resulted in the voltage and current waveforms shown in Figure 5.7. The maximum v_{ac} and i_{load} was simulated to be 31.7 V and 0.317 A. The simulated values were similar to the maximum output voltage and current measured with the prototype. The waveforms shown in Figure 5.7 has similar waveforms to Figure 5.6. Furthermore, the inductor current i_{ems} was observed as shown in Figure 5.8 near the zero voltage crossing point. This current was compared to the simulated i_{ems} as shown in Figure 5.9. It can be seen in both figures that the ripple frequency is approximately 17.5 kHz as expected. The simulation predicts a 1.15 A ripple in i_{ems} and this compares favorably with the actual ripple of 1.26 A at same point. The difference between the simulation results and the measured results can be explained by the current being phase shifted as seen in Figure 5.6. The phase shift is due to the test load not being an ideal pure resistive load as was simulated in the model.

Table 5.1. Summary of parameter values used in the Simulink model.

Parameter	Value	Source
V_{dc}	42.0V	Measured
$V_{control}$ Amplitude	0.832	Prototype
$V_{control}$ Frequency	60 Hz	Prototype
Switching Frequency	17.5 kHz	Prototype
V_{drop}	2 V	[16]
R_{loss}	0.11 Ω	Measured
R_{load}	100 Ω	Measured

The EMS was then measured using unipolar voltage switching mode as shown in Figure 5.10 and simulated in Simulink as shown in Figure 5.11. Once again, the simulation had a comparable maximum voltage and current with the shapes generally matching. The i_{ems} was measured near the zero voltage crossing as shown in Figure 5.12 and compared with the waveform simulated with the model as shown in Figure 5.13. Here it can be seen in both figures that the frequency of the inductor current ripple has doubled to approximately 35 kHz. The doubling in frequency resulted in a reduction of the ripple current due to better filtering from the AC output filter. The peak-to-peak i_{ems} of the simulation was measured to be between 60.6 mA and 111 mA. The actual peak-to-peak values were measured to be 120 mA and 180 mA. The reason for the differences between the Simulink model and the measured values are the same as the bipolar voltage switching case.

The Simulink model has been verified as a good approximation for the H-bridge and AC output filter for both the bipolar and unipolar switching cases. The model can be used to simulate more complex load by switching out the load subsystem block. The model also provides a good base that can be built on to create a more complex model to simulate the DC portion of the EMS. This model could assist with designing and simulating the future EMS controller algorithms.

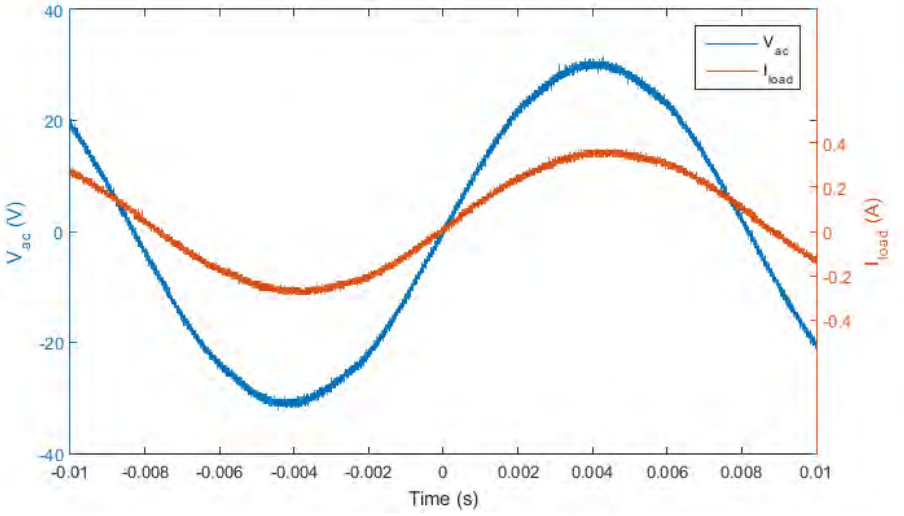

Figure 5.6. The output voltage and current for the actual EMS prototype with bipolar voltage switching and a 100 Ω load.

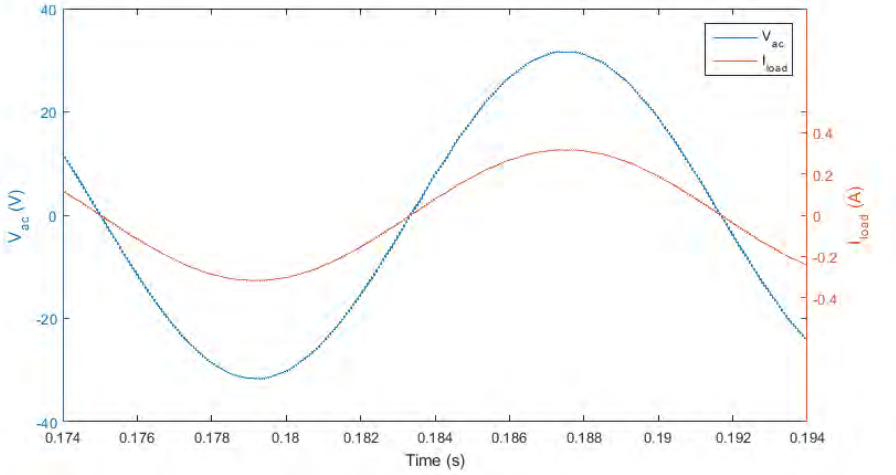

Figure 5.7. The output voltage and current for the simulation with bipolar voltage switching and a 100 Ω load.

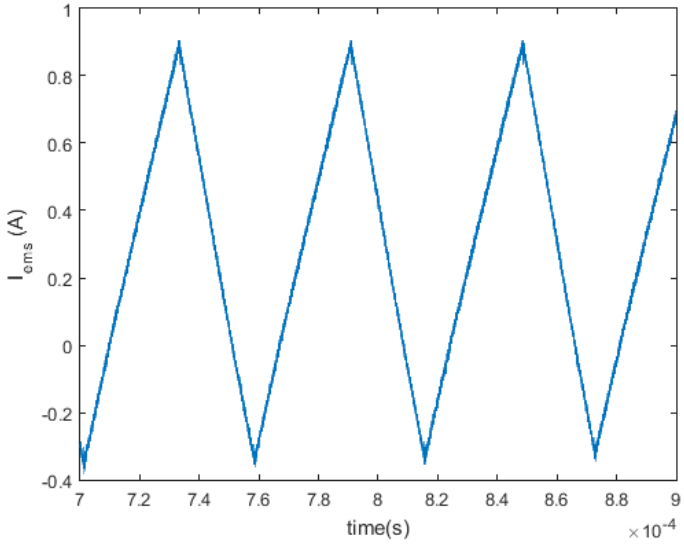

Figure 5.8. The measured inductor current near the zero voltage crossing point while using bipolar switching.

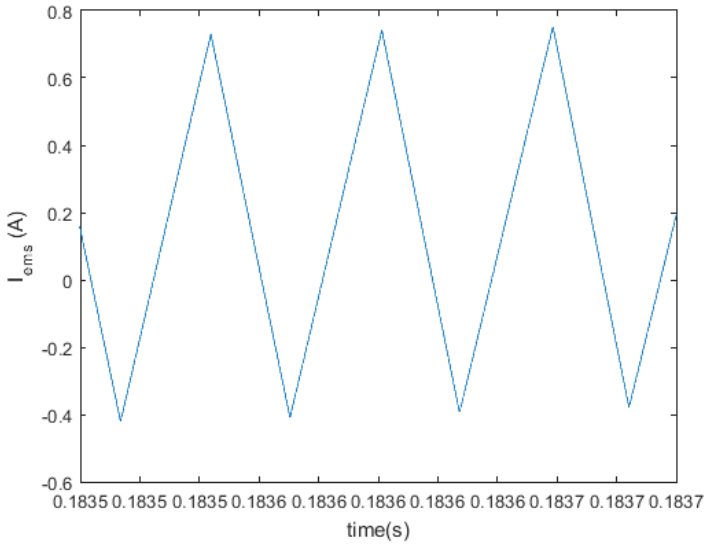

Figure 5.9. The simulated inductor current near the zero voltage crossing point while using bipolar switching.

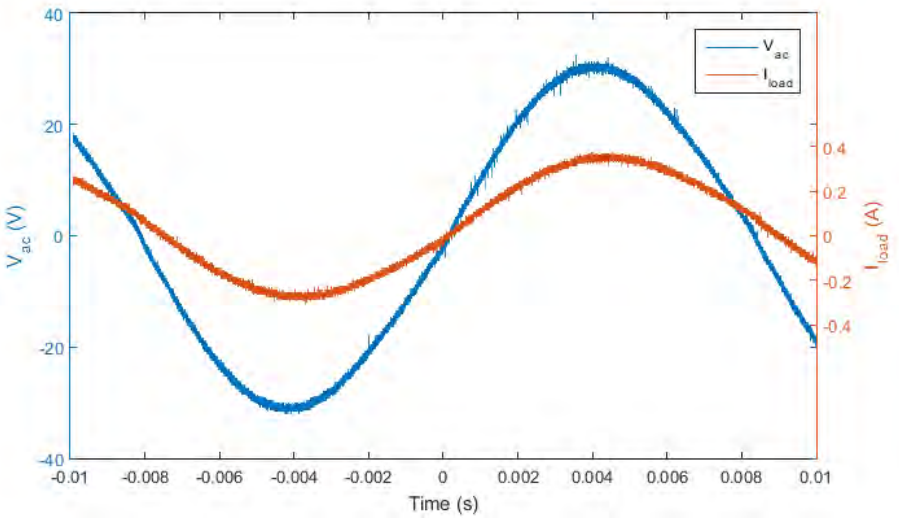

Figure 5.10. The output voltage and current for the actual EMS prototype with unipolar voltage switching and a 100 Ω load.

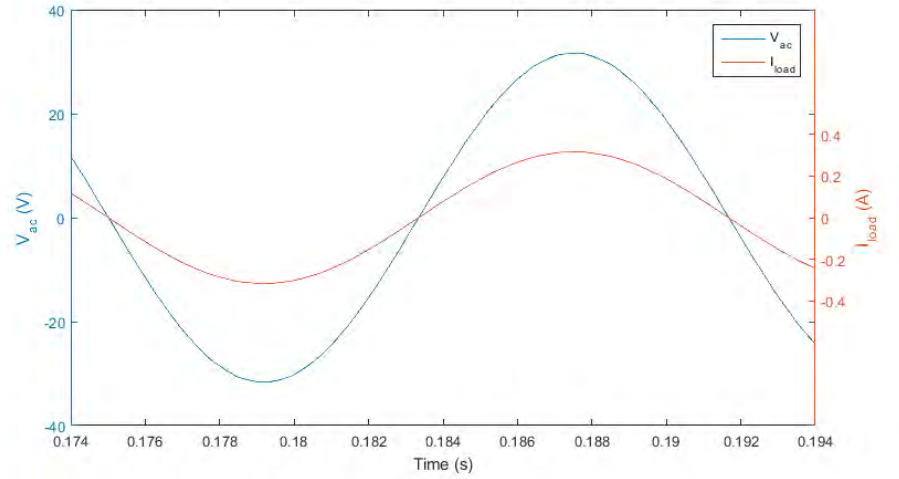

Figure 5.11. The output voltage and current for the simulation with unipolar voltage switching and a 100 Ω load.

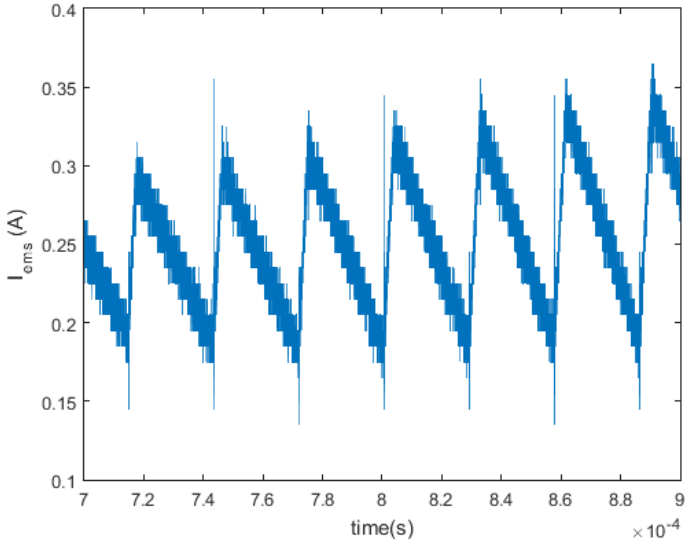

Figure 5.12. The measured inductor current near the zero voltage crossing point while using unipolar switching.

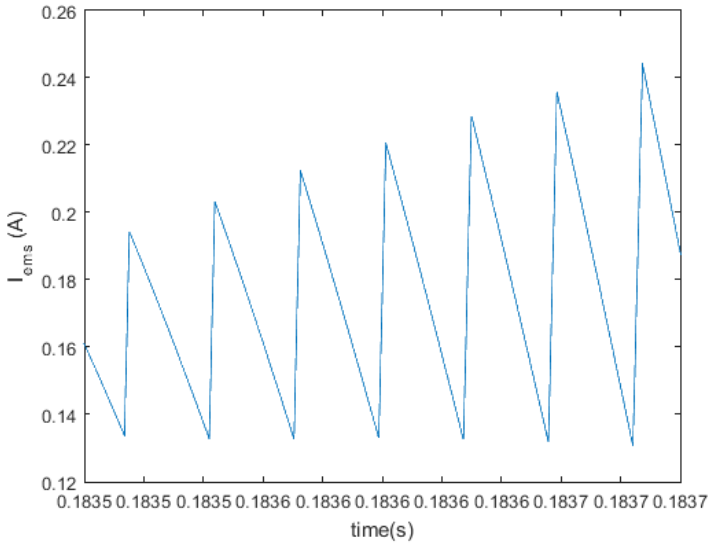

Figure 5.13. The simulated inductor current near the zero voltage crossing point while using unipolar switching.

CHAPTER 6:
Conclusions

A summary of what this thesis accomplishes will be discussed in this chapter. This chapter will also include a discussion of potential future work and recommendations for the 20 A EMS project.

6.1 Summary of Accomplishments

A 20 A EMS prototype was designed and constructed using commercial IGBT power modules. This process included the design of a second-order LC low-pass filter that was used to the filter out switching frequencies from the output. The two inductors for this filter were constructed on a single core and was shown to have approximately double the inductance than if each inductor was wound on its own separate core.

The EMS prototype had some EMI issues due to the switching events that interfered with the operation of the over-current trip portion of the EMS controller. This interference caused the EMS to shutdown on false positives. Two separate digital filters were added to the fault management circuit to filter out the EMI. These filters were designed after it was determined that changes to the analog filter did not make a difference. The first method used was to require three samples from the fault input, taken every 160 ns, to concur before a shutdown signal was generated. The second method was to use a one-bit moving average filter with a sample size of 32 to filter out the noise from the fault signal. Either one of these methods reduced the number of false shutdowns to a minimum.

After the EMI issues were resolved, the over-current trips for the EMS H-bridge power modules were tested. The over-current tests resulted in finding the trip values to be 41.2 A and 44.8 A. These values are different from each other and considerably less than the designed trip values of 50-58 A. The differences are due to the sensitivity of the trip set-points to extra resistance in the PCB tracks.

Finally, a simulation was created in Simulink to model the EMS H-bridge driving a resistive load using both bipolar and unipolar voltage switching schemes. The output voltage and

current were compared to the measured output of the EMS prototype, demonstrating the accuracy of the model. The inductor current from the simulation was also compared to the measured output. The results showed that the Simulink model accurately simulated the inductor current of the EMS. It also showed the reduced ripple current in unipolar versus bipolar switching due to the improved filtering from the LC output filter.

6.2 Future Work

The possible next step for this 20 A EMS prototype would be to work on getting the buck-/boost converter stage working. The buck/boost stage is required to provide an output voltage that matches the 120 VAC grid. Getting this stage to work would require determining the controller parameters and implementing the control loop on the FPGA. The controller should be tested with the three possible DC sources connected to ensure that the controller can handle managing each one separately.

Once this work is complete, additional load testing should be done closer to the design limits. This testing would determine the high current capability of the EMS PCB. The testing should also include inductive loads that would typically be encountered by a functional EMS in the real world.

Finally, the additional features can be added to the Simulink model such as the buck/boost converter and the required control loop. These additions would allow simulations of the controller performance and assist in its design. Also, more complex load models could be added and compared against measured data to refine the model further as needed.

6.3 Recommendations

It is recommended that when a new iteration of the 20 A EMS PCB is designed, a ground plane should be used for the high current portion of the board. Also, separate ground paths for sensitive circuits, such as the over-current fault detection, should be designed with only one path to the main ground plane [19]. These changes would prevent the EMI issues from the current pulse during the switching events from being injected into this sensitive circuitry [19].

Another recommendation is to increase the PCB trace thickness and reduce the trace length

between power modules and the shunt resistors. The same should be done for the traces between the shunt resistors and ground. These changes would minimize the effect of the PCB trace resistance to the over-current trip values for the power modules. This minimization would make the over-current trip set-points closer to the designed values as these set-points are very sensitive to the actual shunt resistance.

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APPENDIX A:
The LTSpice Netlists for AC Output Filter

A.1 Netlist for the Design LC Filter

```
* The 2nd Order LC Filter with the measured total inductance of 235 uH.
* LCDR Matthew McCulley

V1 N001 0 AC 1         $The indepenent AC voltage source
L1 N001 Vout 235u      $The filter Inductor L
C1 Vout 0 12u          $The filter Capacitor C
R1 Vout 0 100          $The load resistor
.ac dec 100 1 50000    $AC frequency sweep from 1Hz to 50 kHz
.backanno
.end
```

A.2 Netlist for the Actual LC Filter

```
* The 2nd Order LC Filter with the measured total inductance off 950 uH.
* LCDR Matthew McCulley

V1 N001 0 AC 1         $The indepenent AC voltage source
L1 N001 Vout 950u      $The filter Inductor L
C1 Vout 0 12u          $The filter Capacitor C
R1 Vout 0 100          $The load resistor
.ac dec 100 1 50000    $AC frequency sweep from 1Hz to 50 kHz
.backanno
.end
```

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APPENDIX B:
MATLAB Code

B.1 The Initial Conditions File for the Simulation

```
% ems_sim_matt_ic.m
% The EMS Simulation Initial Conditions File for 20A EMS Simulation
% LCDR Matthew McCulley
% March 13, 2015

% Clear all variables and close figures
clear all;
close all;

% Simulation Time
tstop=0.2;
% Frequencies
f0 = 60;          %Output Frequency
Vdc=42.0;         %DC Bus Voltage
Vdrop=2;          %IGBT Voltage Drop
V_control=0.832;%The duty cycle for PWM
fsw=17500;        %Switching Frequency
Rload=100;        %Load Resistance

L = 950e-6;       %Output Fiter Inductance
C=12e-6;          %Output Filter Cap
Rloss=0.11;       %Losses in the Output stage

PWM_mode=1;       %PWM_mode 1:Bipolar 0:Unipolar
PWM_on=1;         %Selects to simulate PWM 1: on


% Selects step time based on if simulating PWM
if PWM_on == 0
    tstep = 10e-6;
else
```

```
    tstep = 1e-7;
end
```

B.2 The Plot File for the Simulation

```
% ems_sim_matt_Plot.m
% The EMS Simulation Plot File for 20A EMS Simulation
% LCDR Matthew McCulley

figure(1)
[ax, pl, p2] = plotyy(Time, Vac, Time, Iload);
xlim(ax(1), [.174,.194])
xlim(ax(2), [.174,.194])
ylim(ax(2), [-1, 1])
ylabel(ax(1), 'V_a_c (V)')
ylabel(ax(2), 'I_l_o_a_d (A)')
xlabel(ax(1), 'Time (s)')
legend('V_a_c', 'I_l_o_a_d')

%Iems at zero voltage point
figure(2)
plot(Time, Iems)
xlim([0.1835, 0.1837])
xlabel('time(s)')
ylabel('I_e_m_s (A)')

%Iems at peak voltage
% figure(3)
% plot(Time, Iems)
% xlim([0.1877, 0.1879])
% xlabel('Time(s)')
% ylabel('I_e_m_s (A)')
```

B.3 The Code to Generate the Actual Waveform Plots

```
%% Actual Waveform plots
% Takes the data files from the scope and generates the output voltage and
```

```
% current plots along with the inductor current plots
% Created from auto-generated import code and modified
% LCDR Matthew McCulley

%% Import data from text file.
% Script for importing data from the following text file:
%
%    Tek_CH1_Wfm.csv
%
% To extend the code to different selected data or a different text file,
% generate a function instead of a script.

% Auto-generated by MATLAB on 2015/05/22 12:22:53

%% Initialize variables.
filename = 'Tek_CH1_Wfm.csv';
delimiter = ',';
startRow = 15;

%% Format string for each line of text:
%   column1: double (%f)
%   column2: double (%f)
% For more information, see the TEXTSCAN documentation.
formatSpec = '%f%f%[^\n\r]';

%% Open the text file.
fileID = fopen(filename,'r');

%% Read columns of data according to format string.
% This call is based on the structure of the file used to generate this
% code. If an error occurs for a different file, try regenerating the code
% from the Import Tool.
textscan(fileID, '%[^\n\r]', startRow-1, 'ReturnOnError', false);
dataArray = textscan(fileID, formatSpec, 'Delimiter', delimiter, 'EmptyValue',...
NaN,'ReturnOnError', false);

%% Close the text file.
fclose(fileID);
```

```
%% Post processing for unimportable data.
% No unimportable data rules were applied during the import, so no post
% processing code is included. To generate code which works for
% unimportable data, select unimportable cells in a file and regenerate the
% script.

%% Allocate imported array to column variable names
T_act_1 = dataArray{:, 1};
Vac_act = dataArray{:, 2};


%% Clear temporary variables
clearvars filename delimiter startRow formatSpec fileID dataArray ans;

%% Import data from text file.
% Script for importing data from the following text file:
%
%    Tek_CH2_Wfm.csv
%
% To extend the code to different selected data or a different text file,
% generate a function instead of a script.

% Auto-generated by MATLAB on 2015/05/22 12:24:19

%% Initialize variables.
filename = 'Tek_CH2_Wfm.csv';
delimiter = ',';
startRow = 15;

%% Format string for each line of text:
%   column1: double (%f)
%   column2: double (%f)
% For more information, see the TEXTSCAN documentation.
formatSpec = '%f%f%[^\n\r]';

%% Open the text file.
fileID = fopen(filename,'r');

%% Read columns of data according to format string.
```

```
% This call is based on the structure of the file used to generate this
% code. If an error occurs for a different file, try regenerating the code
% from the Import Tool.
textscan(fileID, '%[^\n\r]', startRow-1, 'ReturnOnError', false);
dataArray = textscan(fileID, formatSpec, 'Delimiter', delimiter, 'EmptyValue',...
    NaN,'ReturnOnError', false);

%% Close the text file.
fclose(fileID);

%% Post processing for unimportable data.
% No unimportable data rules were applied during the import, so no post
% processing code is included. To generate code which works for
% unimportable data, select unimportable cells in a file and regenerate the
% script.

%% Allocate imported array to column variable names
T_act_2 = dataArray{:, 1};
Iload_act = dataArray{:, 2};


%% Clear temporary variables
clearvars filename delimiter startRow formatSpec fileID dataArray ans;


%% Import data from text file.
% Script for importing data from the following text file:
%
%    Tek_CH2_Wfm_Inductor_Current_Zero_Point.csv
%
% To extend the code to different selected data or a different text file,
% generate a function instead of a script.

% Auto-generated by MATLAB on 2015/05/22 12:34:50

%% Initialize variables.
filename = 'Tek_CH2_Wfm_Inductor_Current_Zero_Crossing.csv';
delimiter = ',';
startRow = 15;
```

```
%% Format string for each line of text:
%   column1: double (%f)
%   column2: double (%f)
% For more information, see the TEXTSCAN documentation.
formatSpec = '%f%f%[^\n\r]';

%% Open the text file.
fileID = fopen(filename,'r');

%% Read columns of data according to format string.
% This call is based on the structure of the file used to generate this
% code. If an error occurs for a different file, try regenerating the code
% from the Import Tool.
textscan(fileID, '%[^\n\r]', startRow-1, 'ReturnOnError', false);
dataArray = textscan(fileID, formatSpec, 'Delimiter', delimiter, 'EmptyValue',...
    NaN,'ReturnOnError', false);

%% Close the text file.
fclose(fileID);

%% Post processing for unimportable data.
% No unimportable data rules were applied during the import, so no post
% processing code is included. To generate code which works for
% unimportable data, select unimportable cells in a file and regenerate the
% script.

%% Allocate imported array to column variable names
T_act_3 = dataArray{:, 1};
I_ems_act_zero = dataArray{:, 2};


%% Clear temporary variables
clearvars filename delimiter startRow formatSpec fileID dataArray ans;



%% Plots for Actual Waveforms
figure(3)
```

```
[ax, pl, p2] = plotyy(T_act_1, Vac_act, T_act_2, Iload_act);
xlim(ax(1), [-0.01,0.01])
xlim(ax(2), [-0.01,0.01])
ylim(ax(1), [-40,40])
ylim(ax(2), [-1, 1])
ylabel(ax(1), 'V_a_c (V)')
ylabel(ax(2), 'I_l_o_a_d (A)')
xlabel(ax(1), 'Time (s)')
legend('V_a_c', 'I_l_o_a_d')

figure(4)
plot(T_act_3, I_ems_act_zero)
xlabel('time(s)')
ylabel('I_e_m_s (A)')
```

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